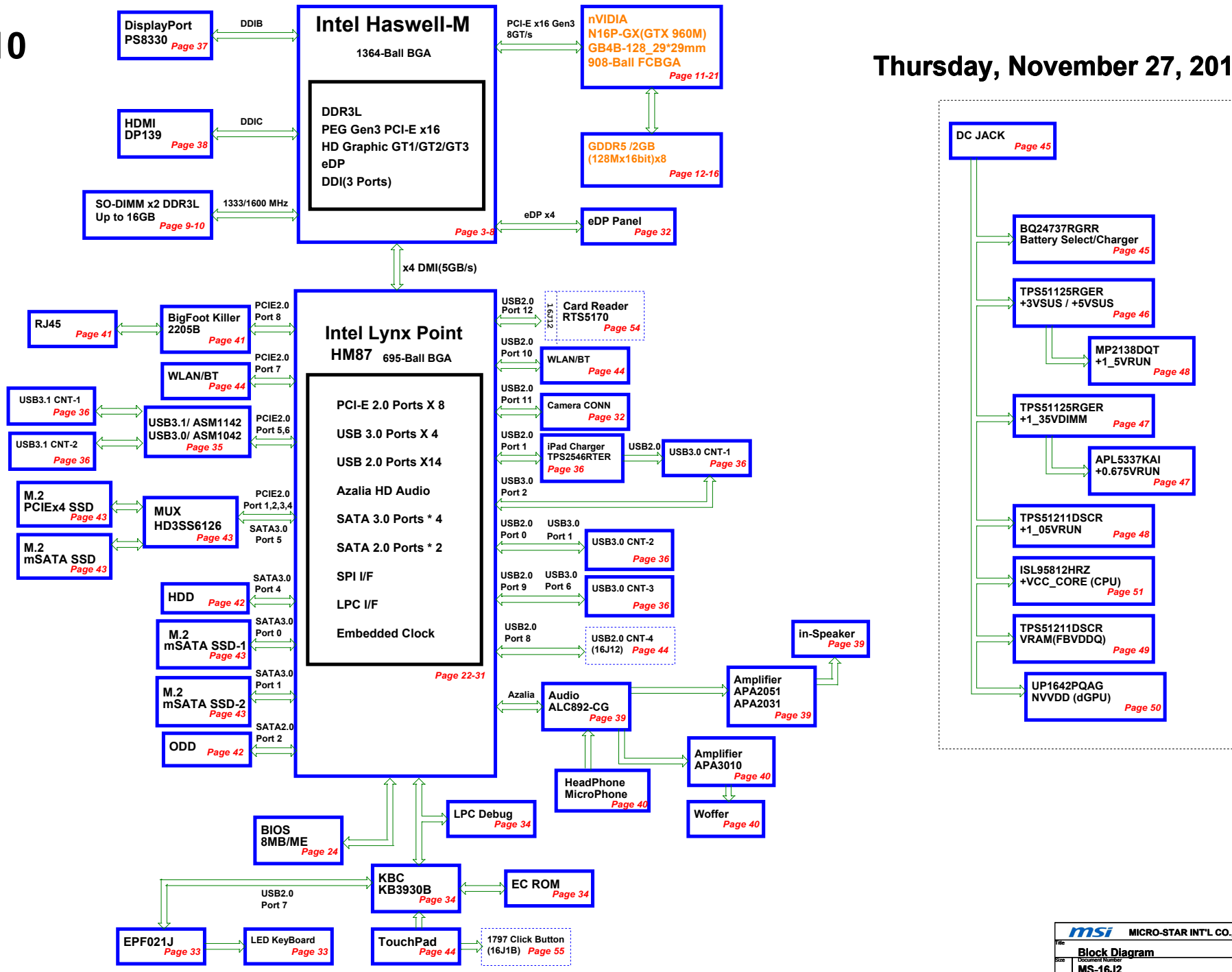


# MS-16J2 /1792

Ver:10

## Shark Bay Mobile

Thursday, November 27, 2014



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

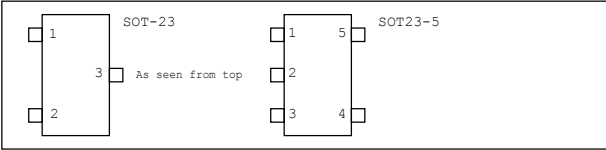
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVDD	V Core Voltage for nVIDIA dGPU	NVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVDD_EN

Net Naming Conventions

<b>Suffix</b>
# = Active Low Signal
<b>Prefix</b>
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx = Like Test Point, but using VIA.

PCB Footprints



<b>BOM</b>	607-16J21-01S	607-16J21-02S	607-17921-01S	607-17921-02S
<b>CPU</b>	I7-4720HQ	I7-4720HQ	I7-4720HQ	I7-4720HQ
<b>Graphics</b>	N16P-GX(GTX960M)	N16P-GX(GTX960M)	N16P-GX(GTX960M)	N16P-GX(GTX960M)
<b>MB ID</b>	PR147 100K pull-up	PR147 100K pull-up	PR147 100K pull-up	PR147 100K pull-up
<b>GDDR5</b>	Hynix H5GC2H24BFR-T2C M12-5GC2H05-H23	Micron EDW2032BBBG-6A-F M12-2032B95-M30	Hynix H5GC2H24BFR-T2C M12-5GC2H05-H23	Micron EDW2032BBBG-6A-F M12-2032B95-M30
<b>STRAP</b>	R3082 10K 1% PD R11-0103T12-W08	R3082 30.1K 1% PD R11-3012T12-W08	R3082 10K 1% PD R11-0103T12-W08	R3082 30.1K 1% PD R11-3012T12-W08
<b>SW&amp;LED</b>	Stuff UB1  SW1,SW2, R479,R480,R481,R482, D9,D10,D11,D12 D1  device on board A and B don't stuff		Stuff UB2  FPC17,FPCB1,SWB3,SWB4 RB479,RB480,RB481,RB482 DB9,DB10,DB11,DB12 D14	

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0( Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V\*SUS always keep high

# Haswell ( DMI,PEG,FDI )

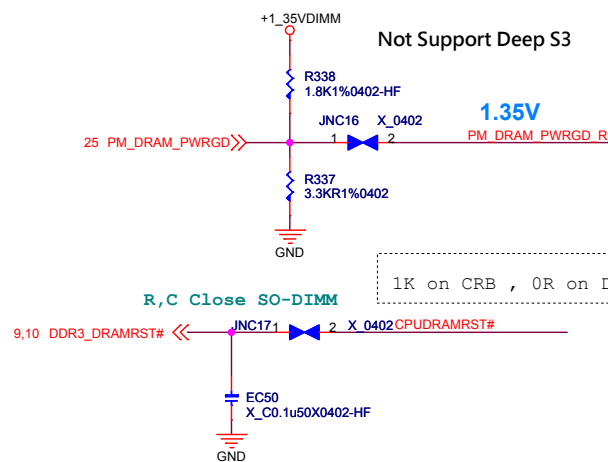
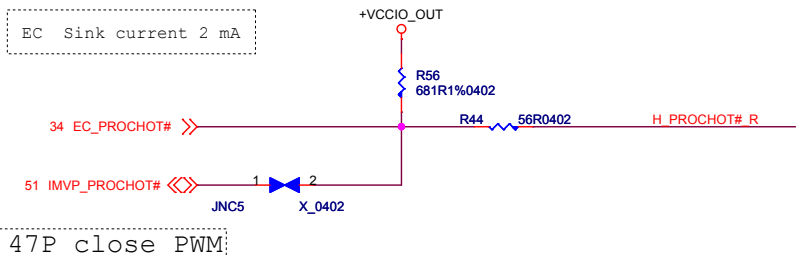
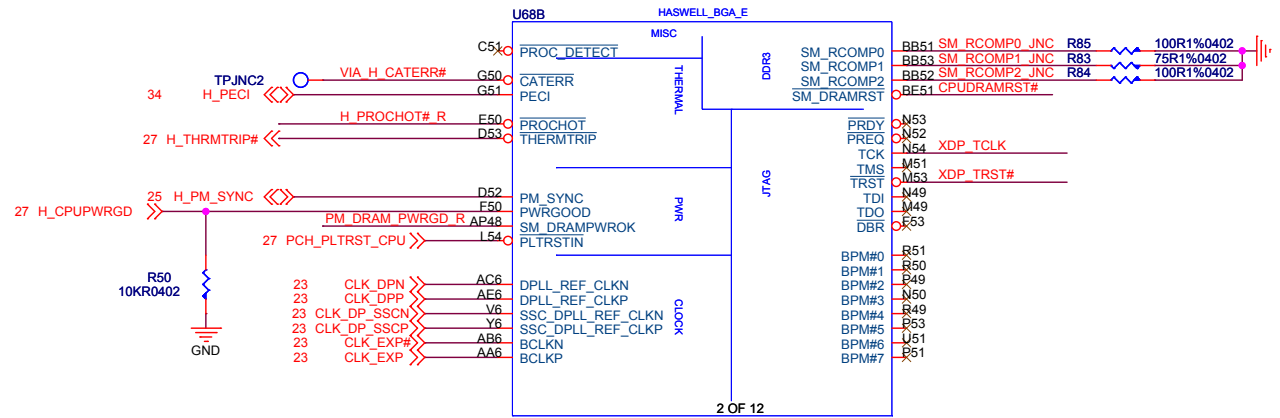
PEG\_RCOMP  
Width:12 mils  
Spacing:15 mils  
Length:400 mils



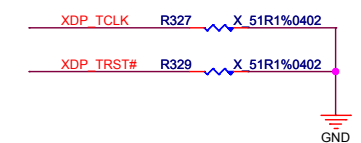
# Haswell ( CLK,MISC,JTAG )

i7-4710HQ, (SR1PX) , 2.5GHz

SM\_RCOMP\_0/1/2 : 15/20/25/15/20/25  
SM\_RCOMP\_0/1/2 Length max: 500mil



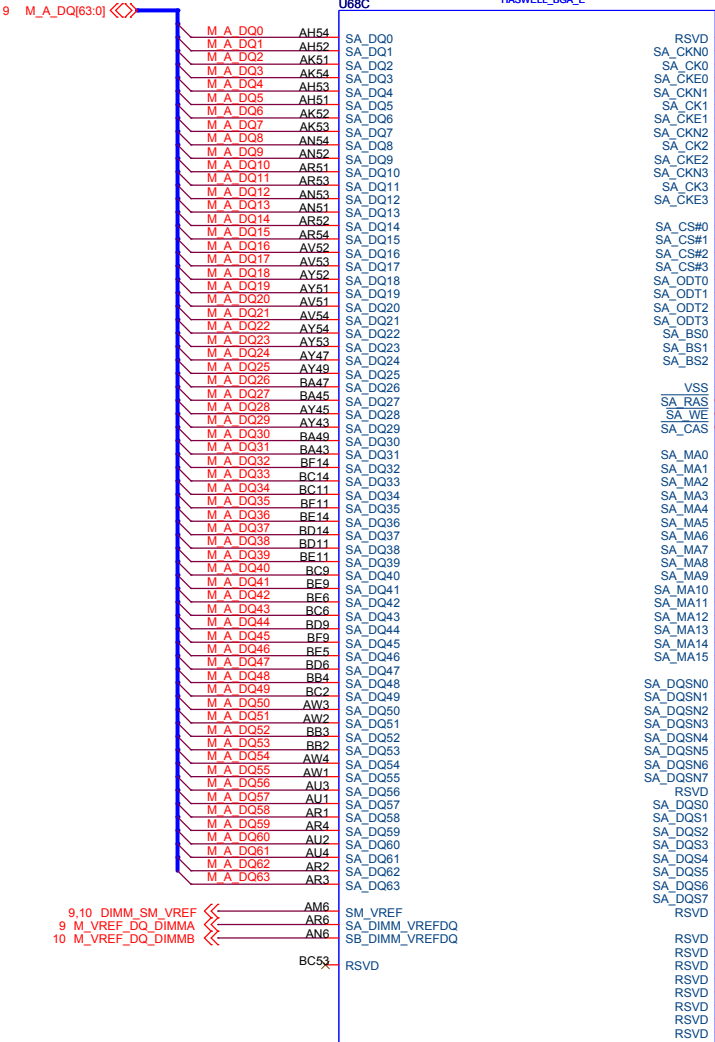
p.11 479493\_479493\_SharkBay\_HSW\_ext\_rev2.0.pdf  
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREG# and PRDY# signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.



Haswell ( DDR3L )

SODIMM#A

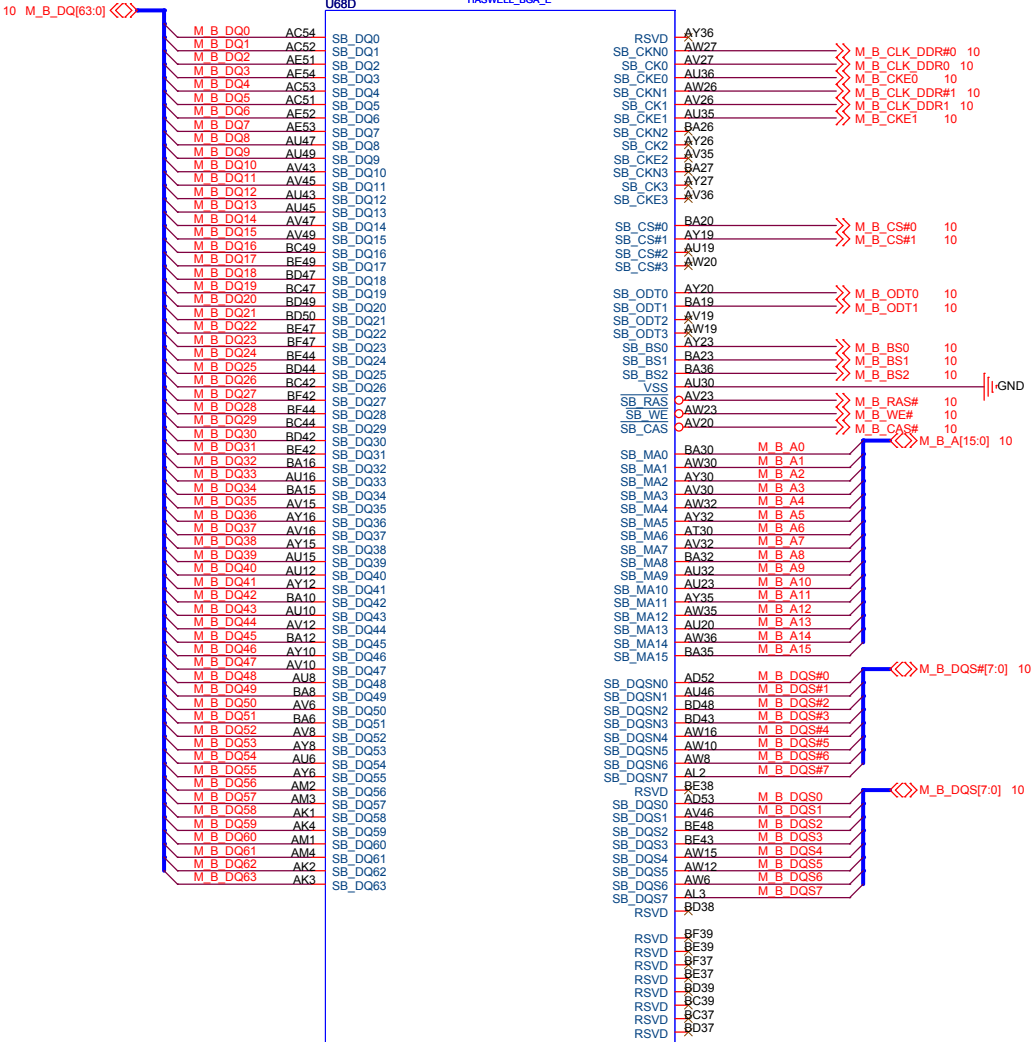
HASWELL\_BGA\_E



3 OF 12

SODIMM#B

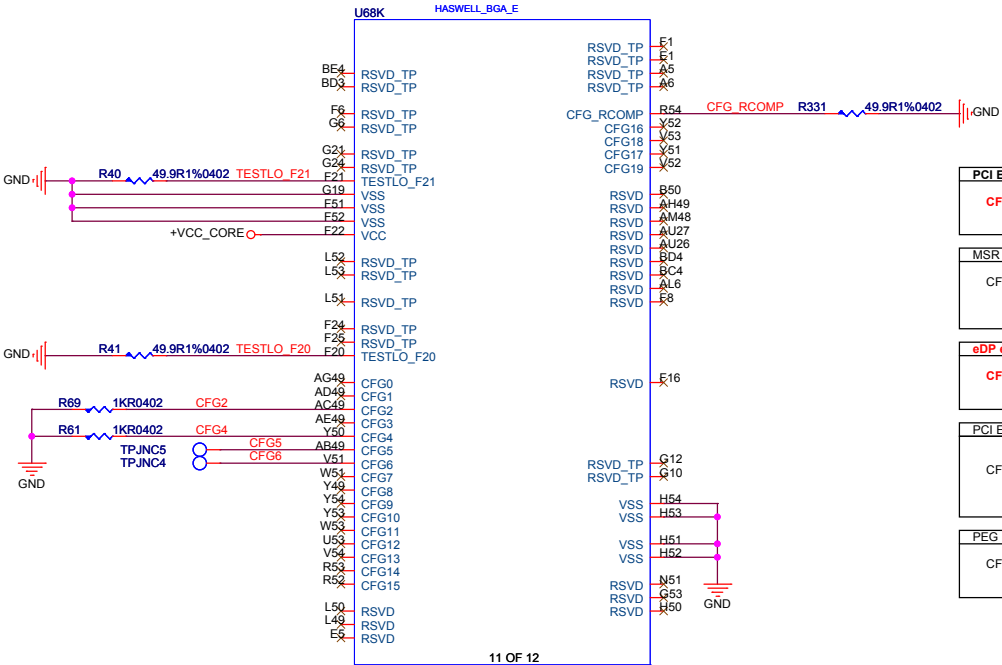
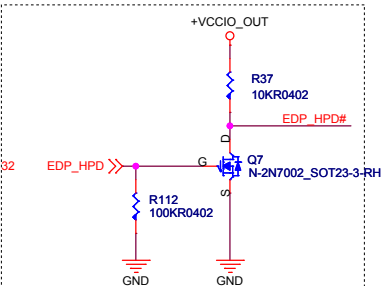
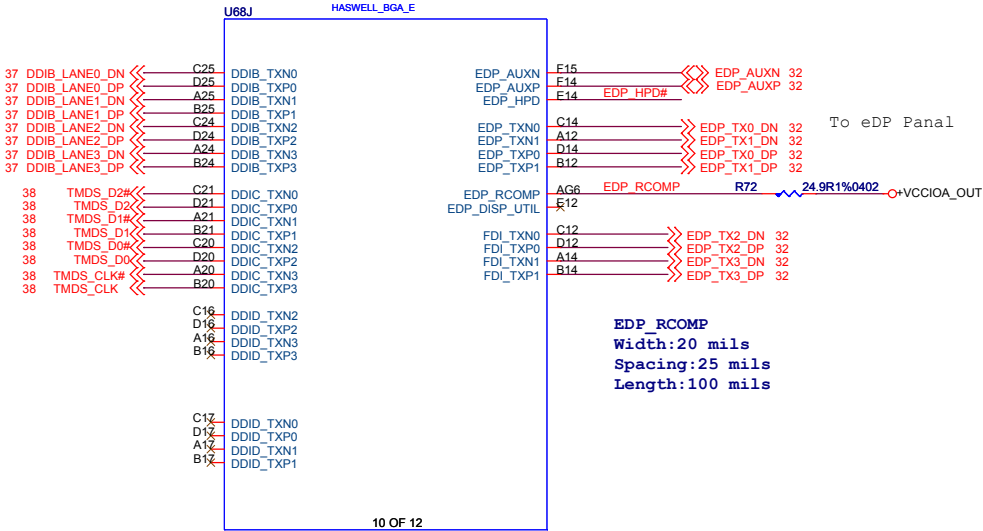
HASWELL\_BGA\_E



4 OF 12

Display/Reserved

DP  
HDMI



PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

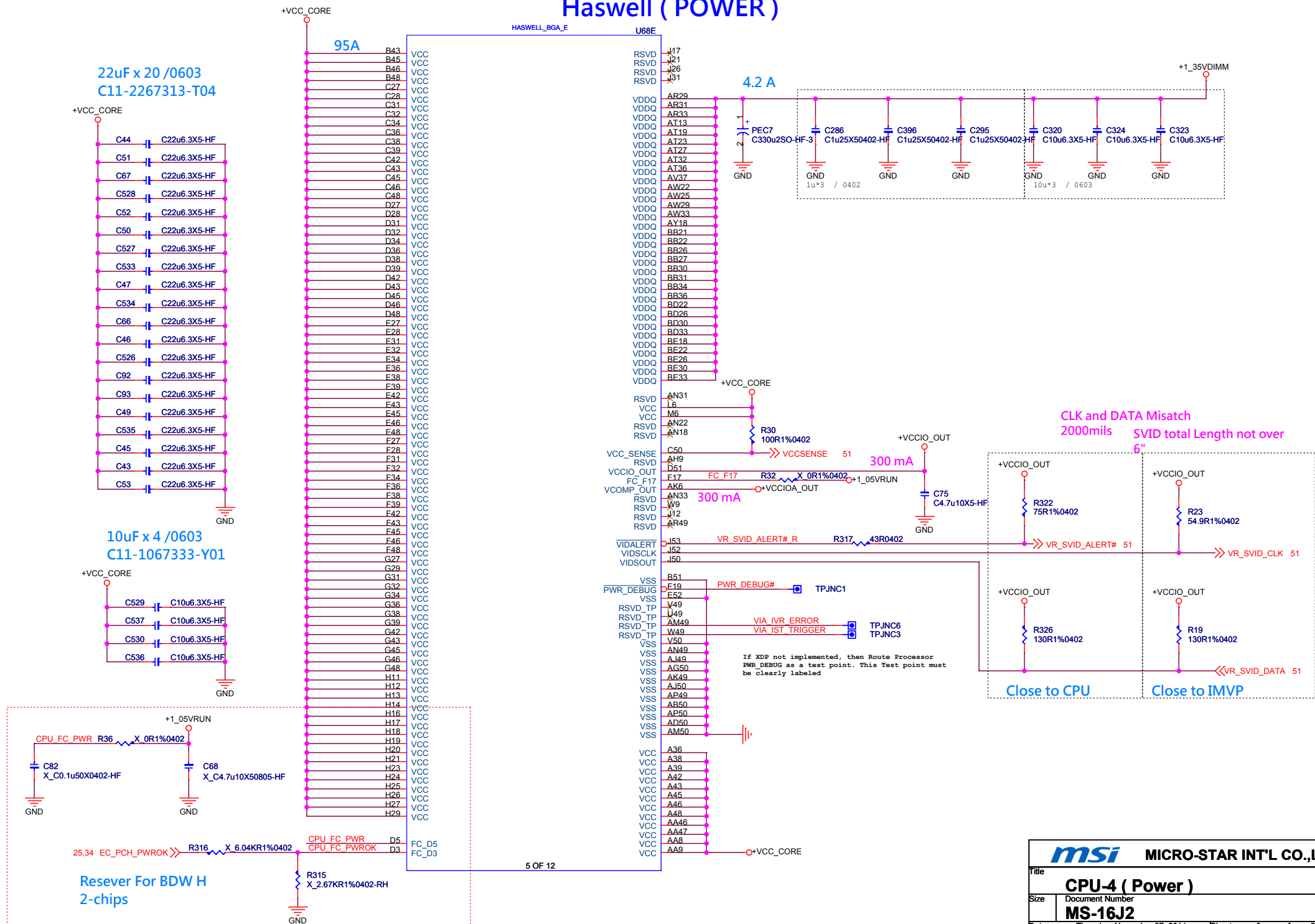
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

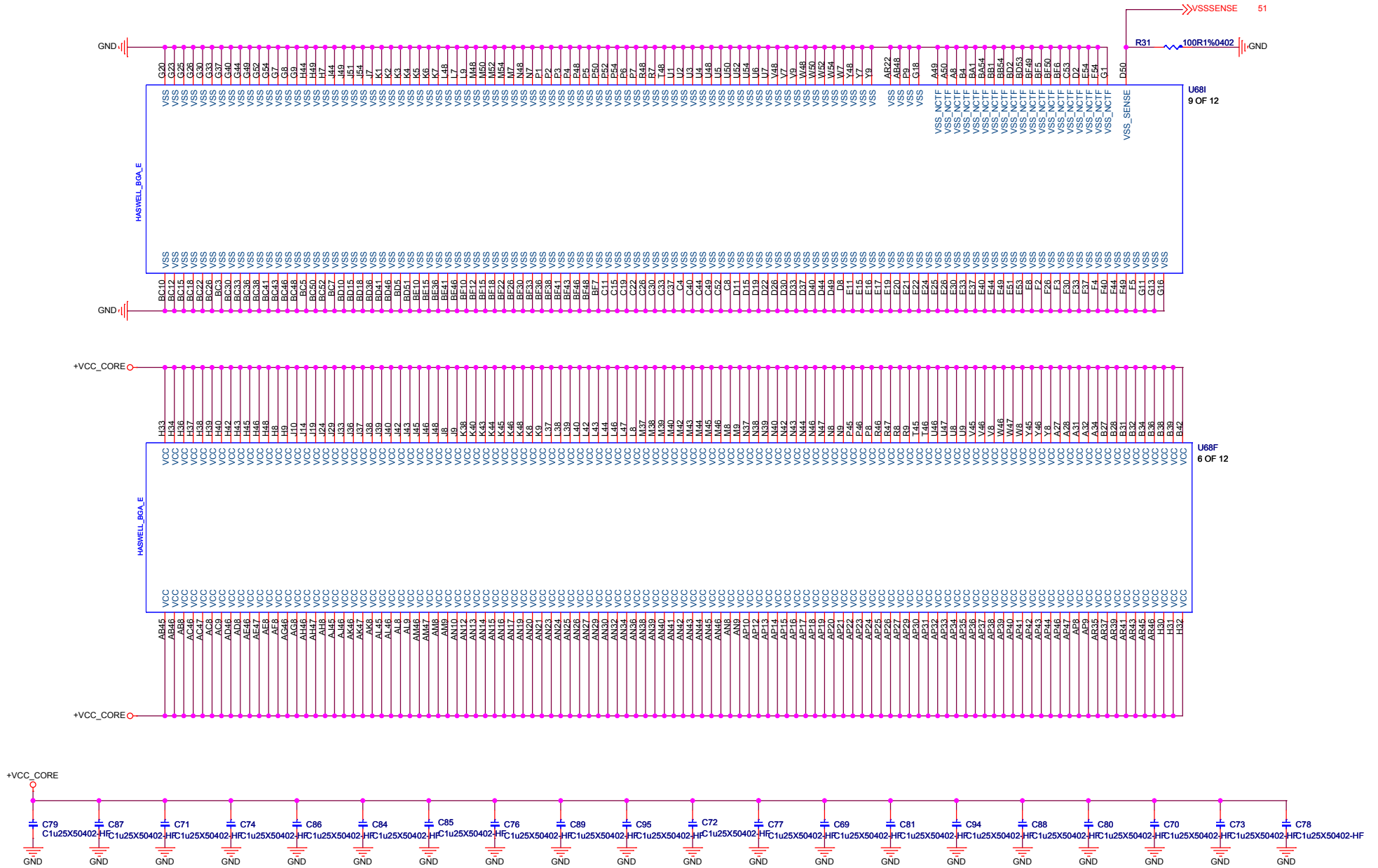
PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

## Haswell ( POWER )

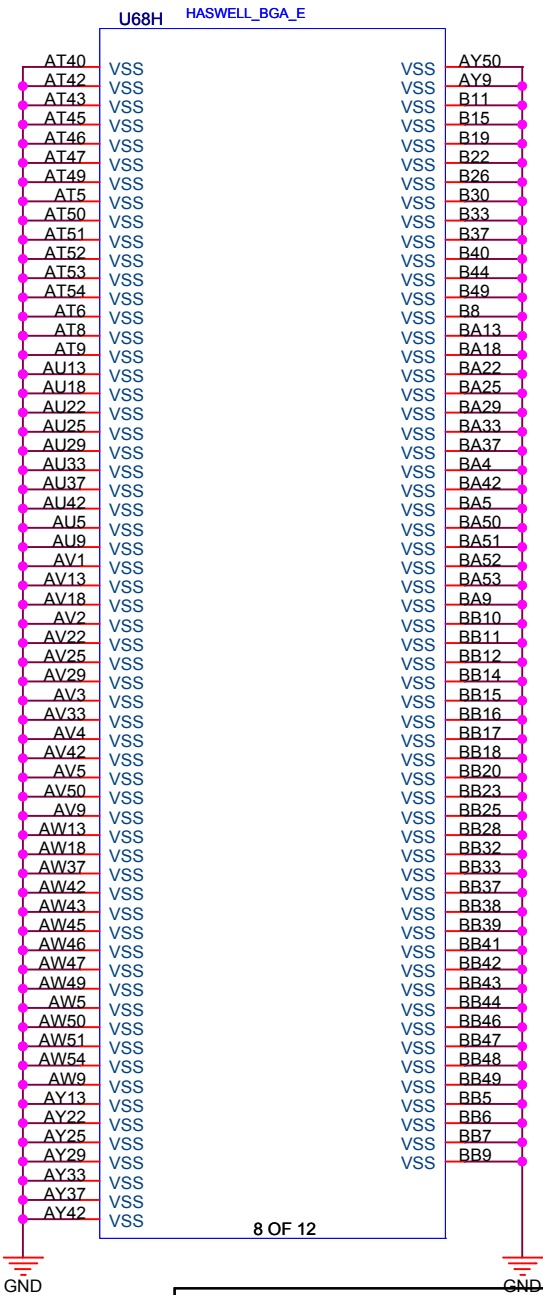
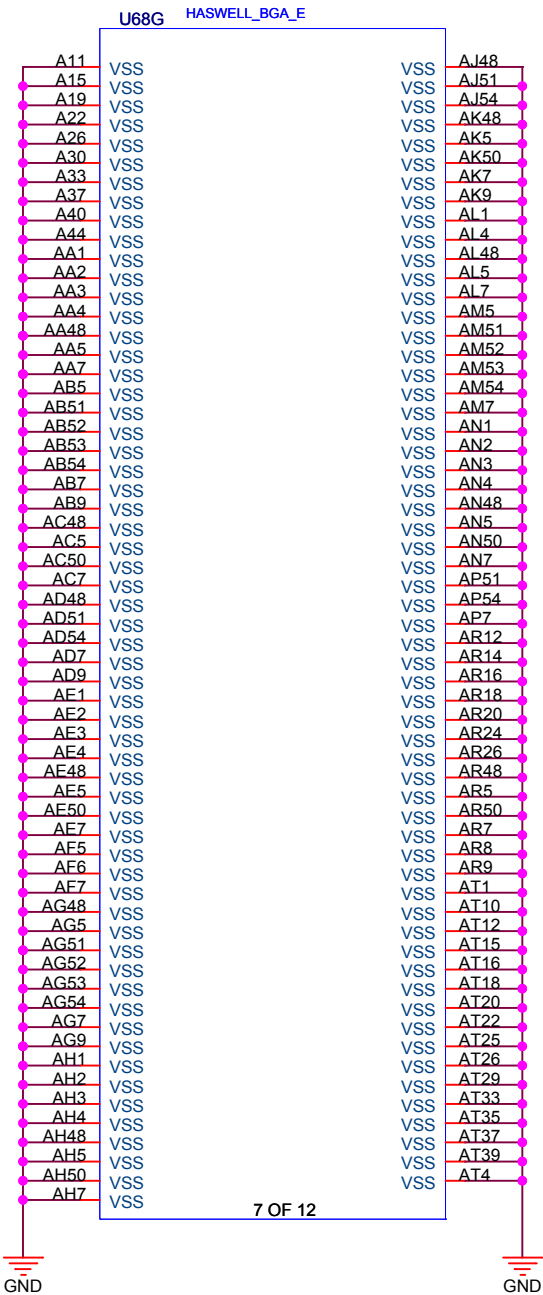



# Haswell ( Power & GND )





Haswell ( GND )



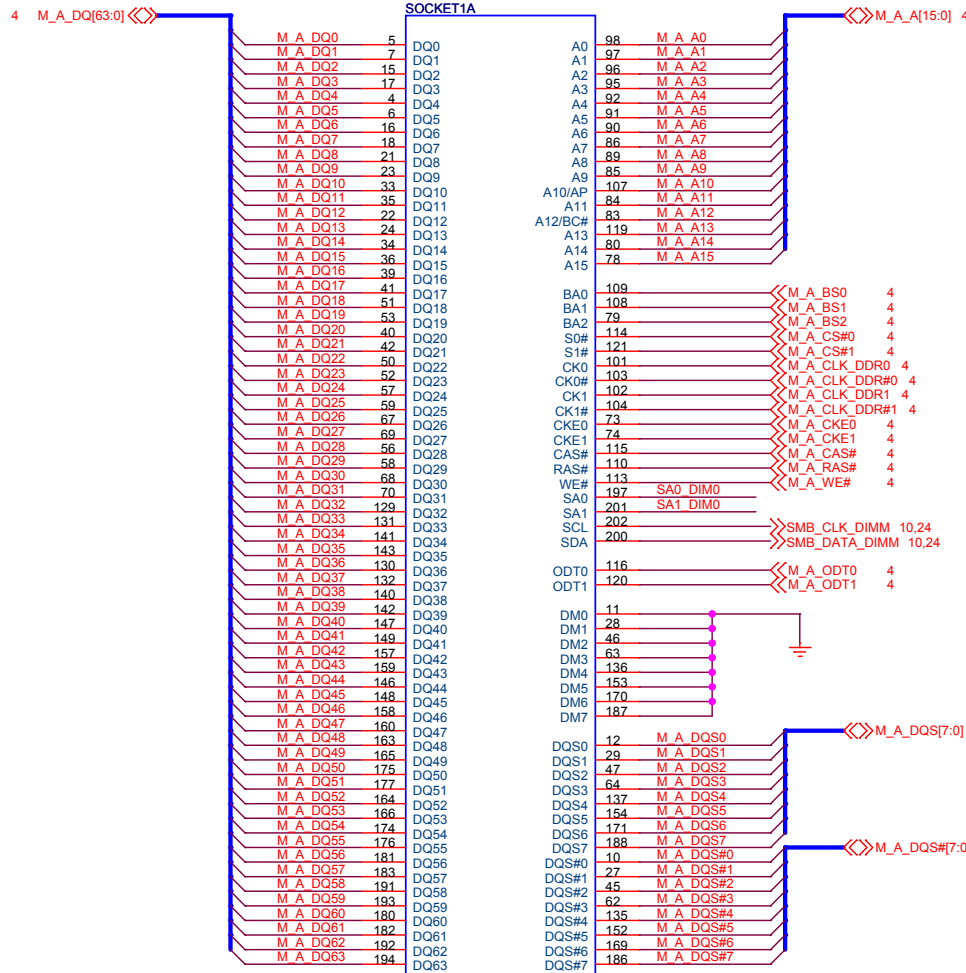


MICRO-STAR INT'L CO.,LTD.

Title		
CPU-5 ( GND )		
Size	Document Number	Rev
	MS-16J2	10
Date:	Thursday, November 27, 2014	Sheet 8 of 59

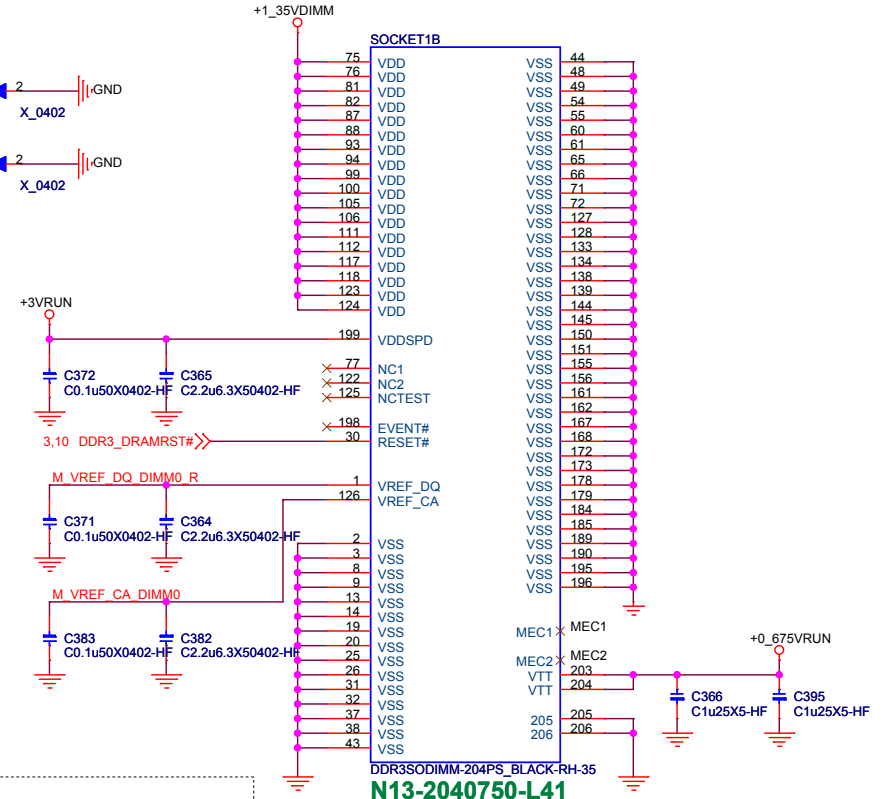
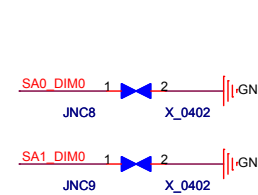
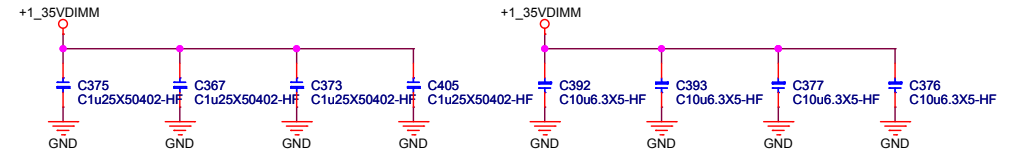


# SODIMM#A



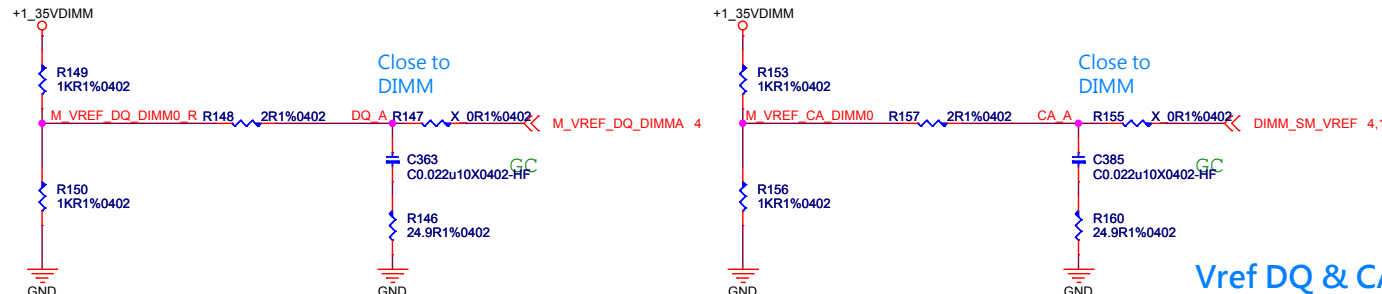
REV. N13-2040750-L41

M1 (used for S3)  
M3 (used for S0), maybe to over-ride  
Active when soft-start



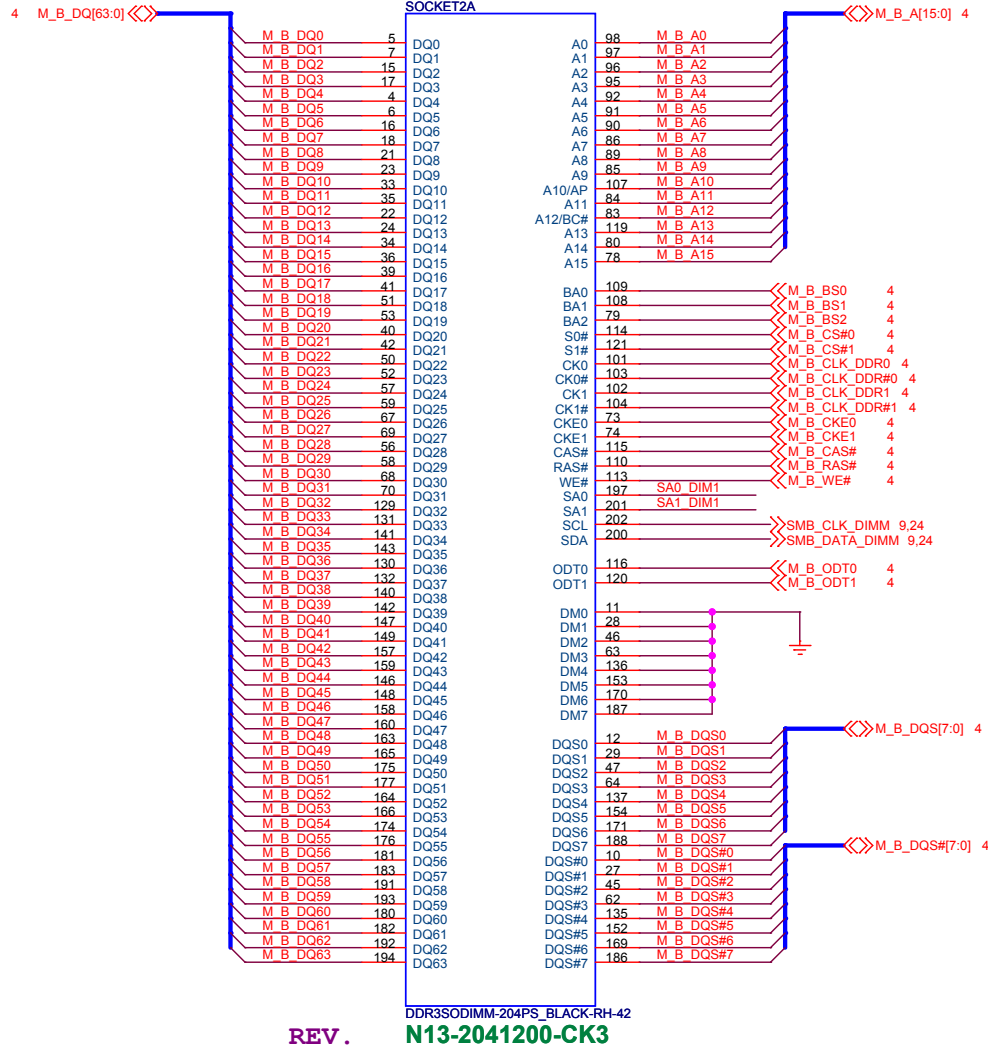
DDR3SODIMM-204PS\_BLACK-RH-35

N13-2040750-L41

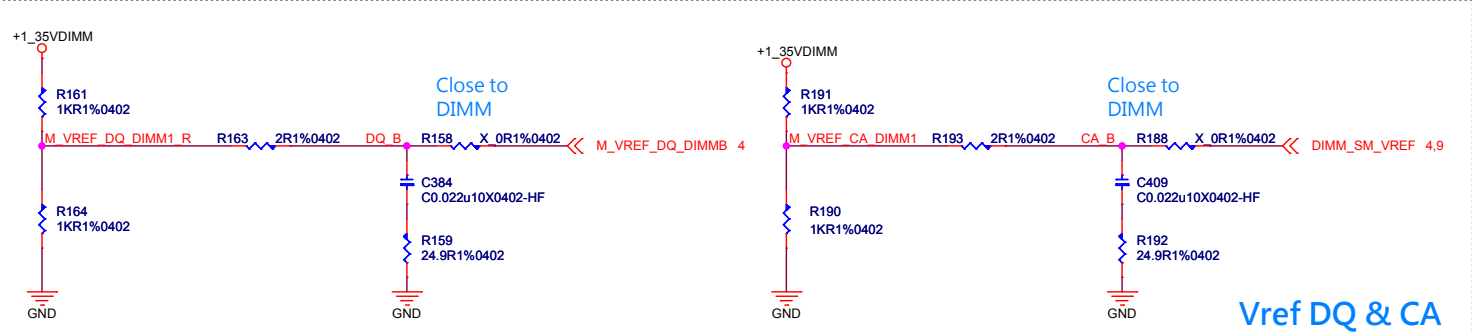
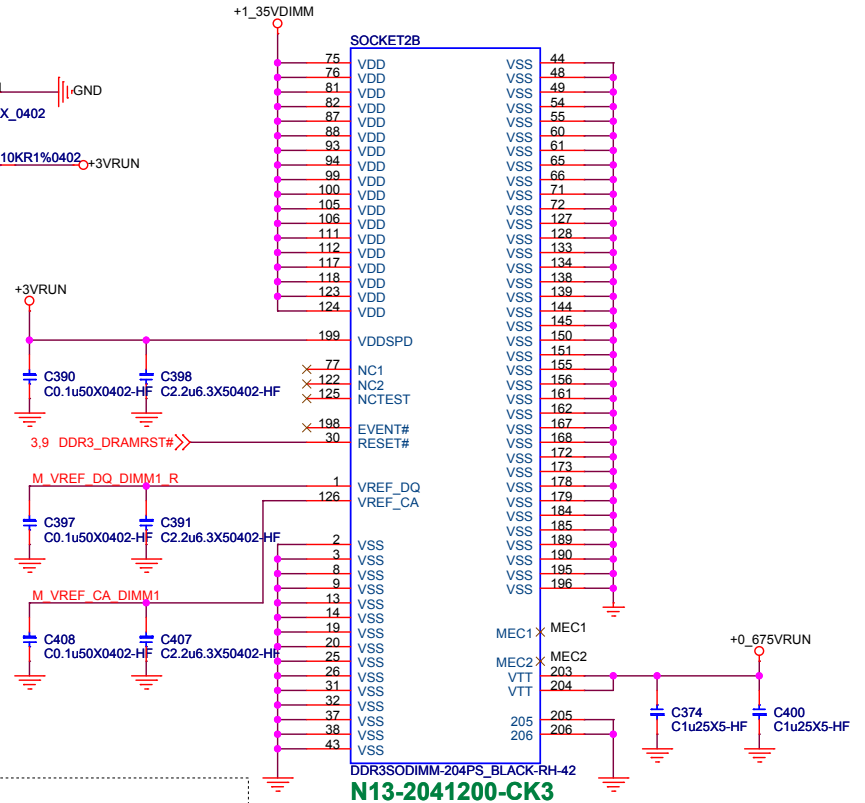
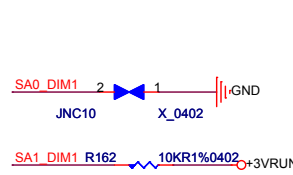
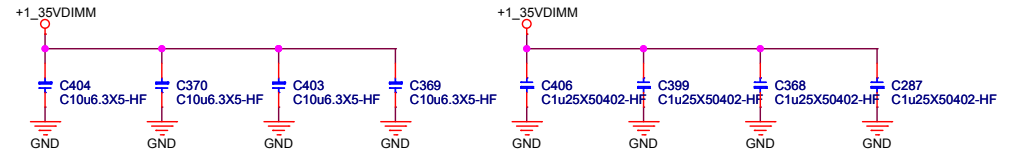


Vref DQ & CA

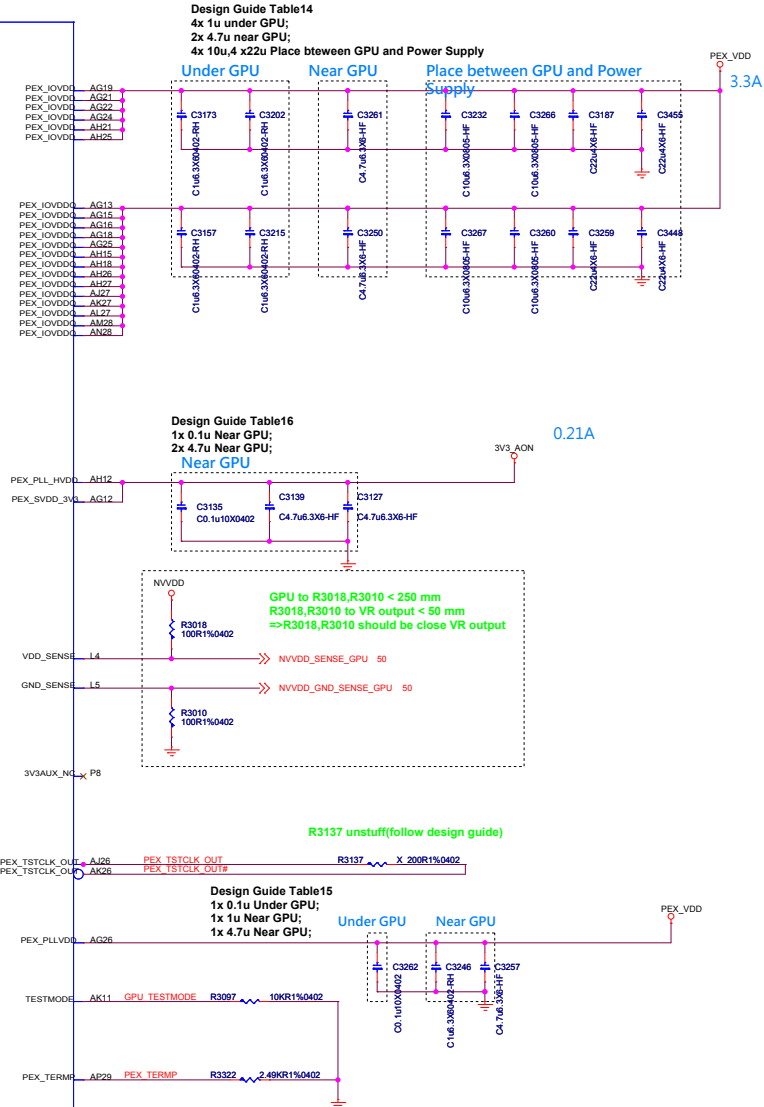
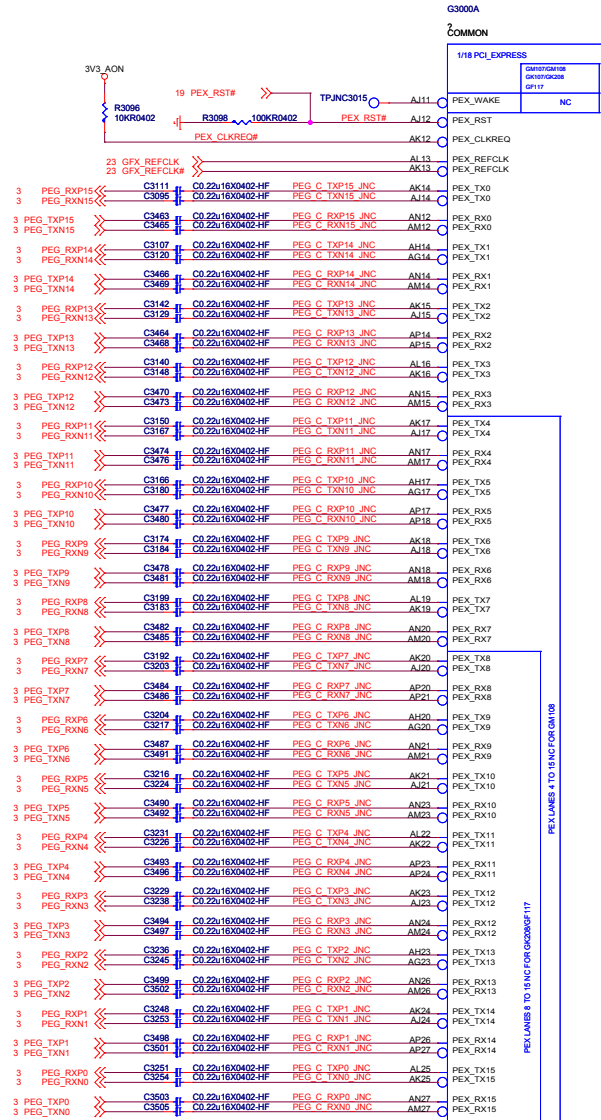
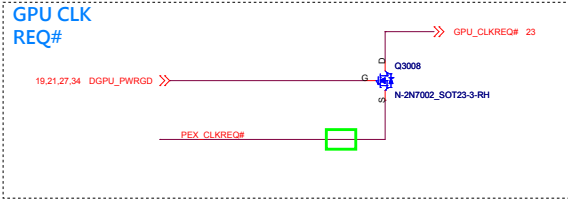
# SODIMM#B



REV. N13-2041200-CK3

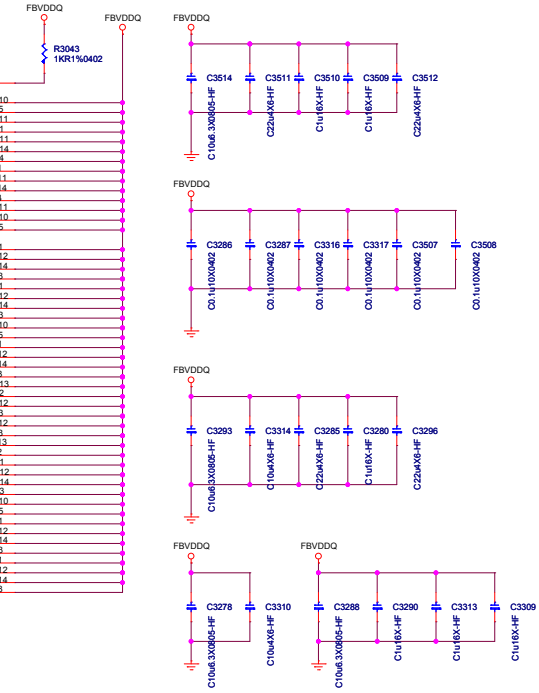
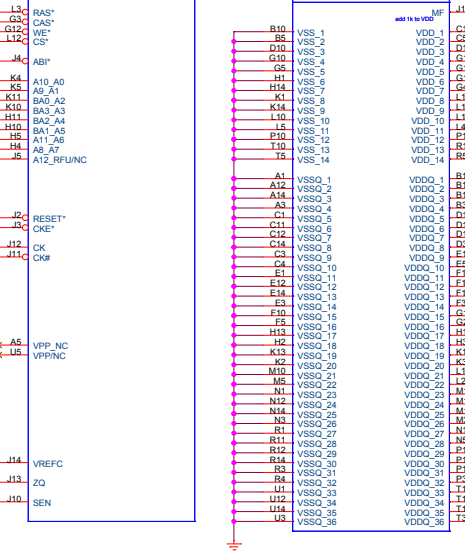
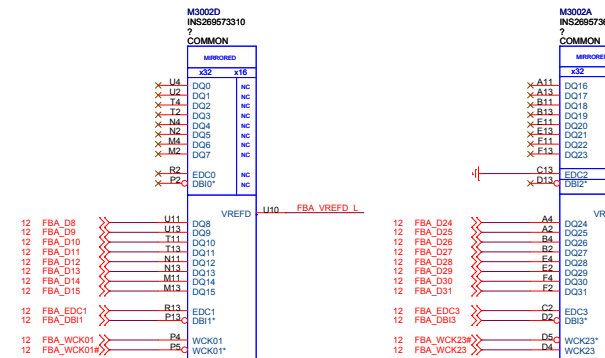
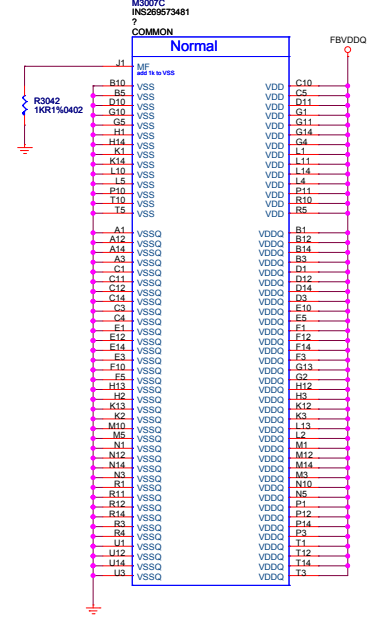
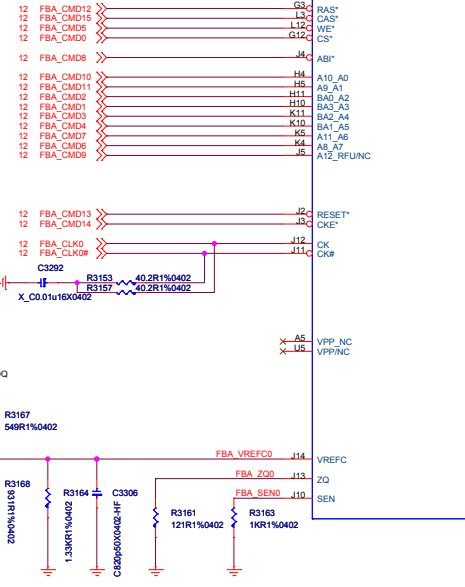
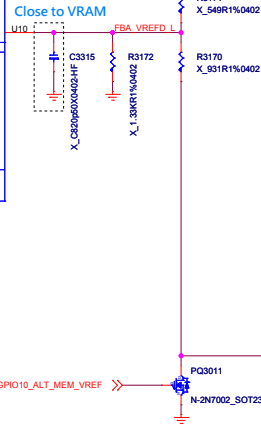
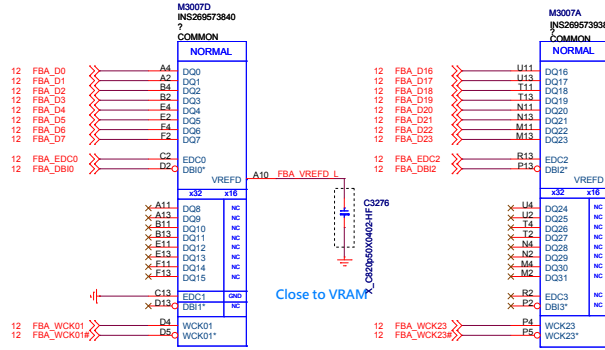


N16P-GX( PCI-Express Gen3 x16 Interface)

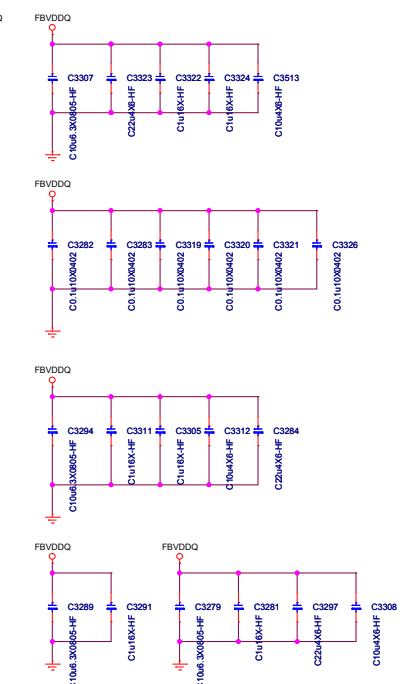
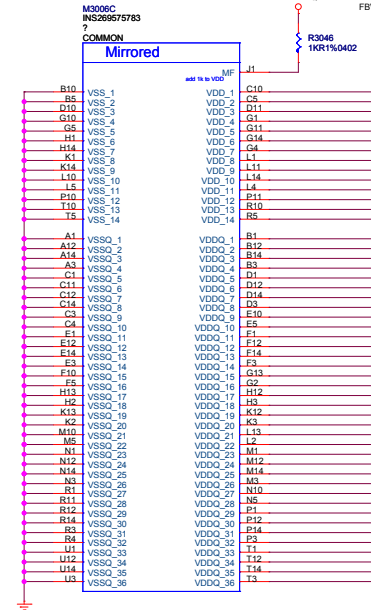
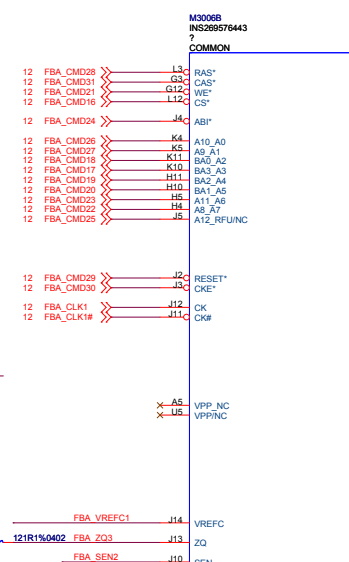
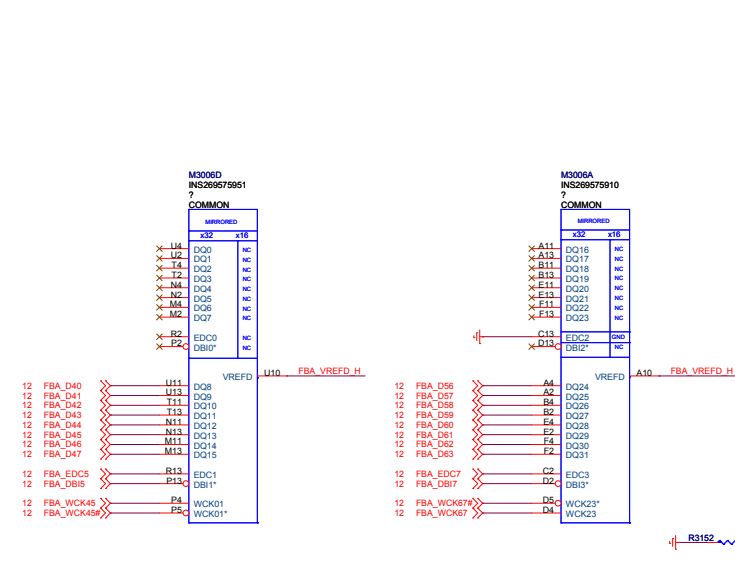
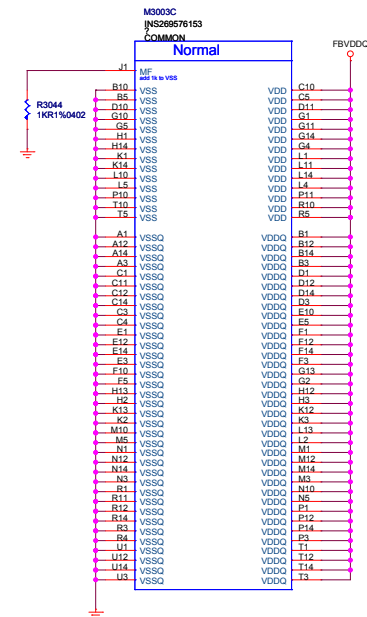
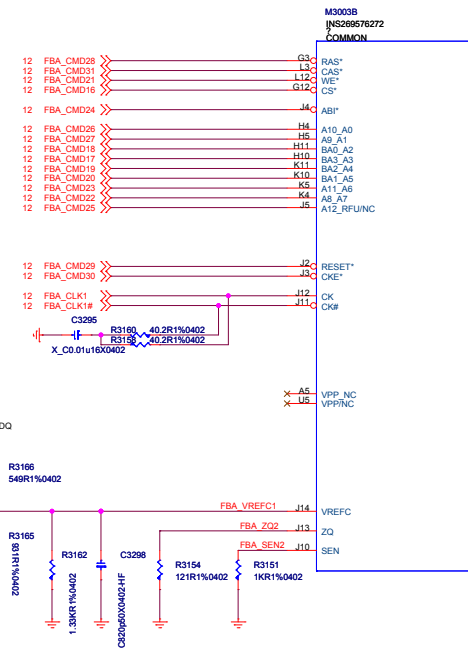
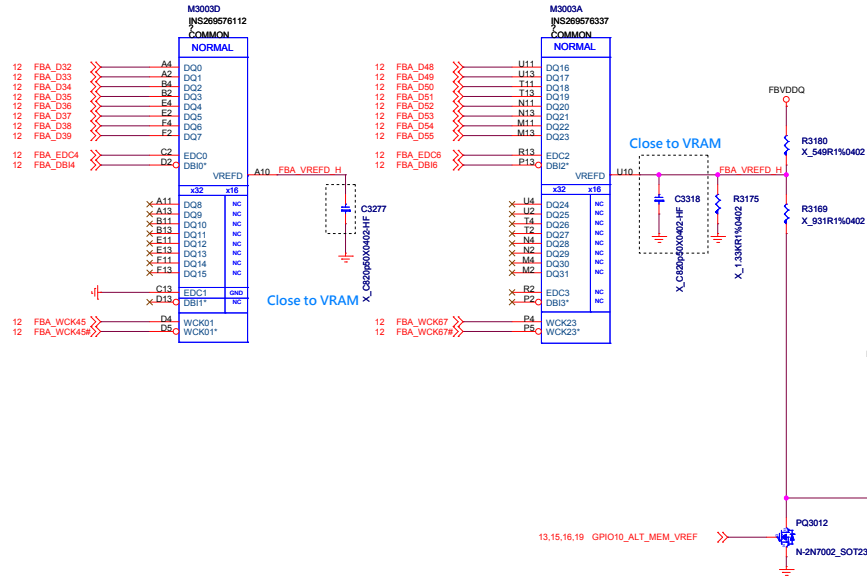




# N16P-GX( GDDR5 Frame A-1)

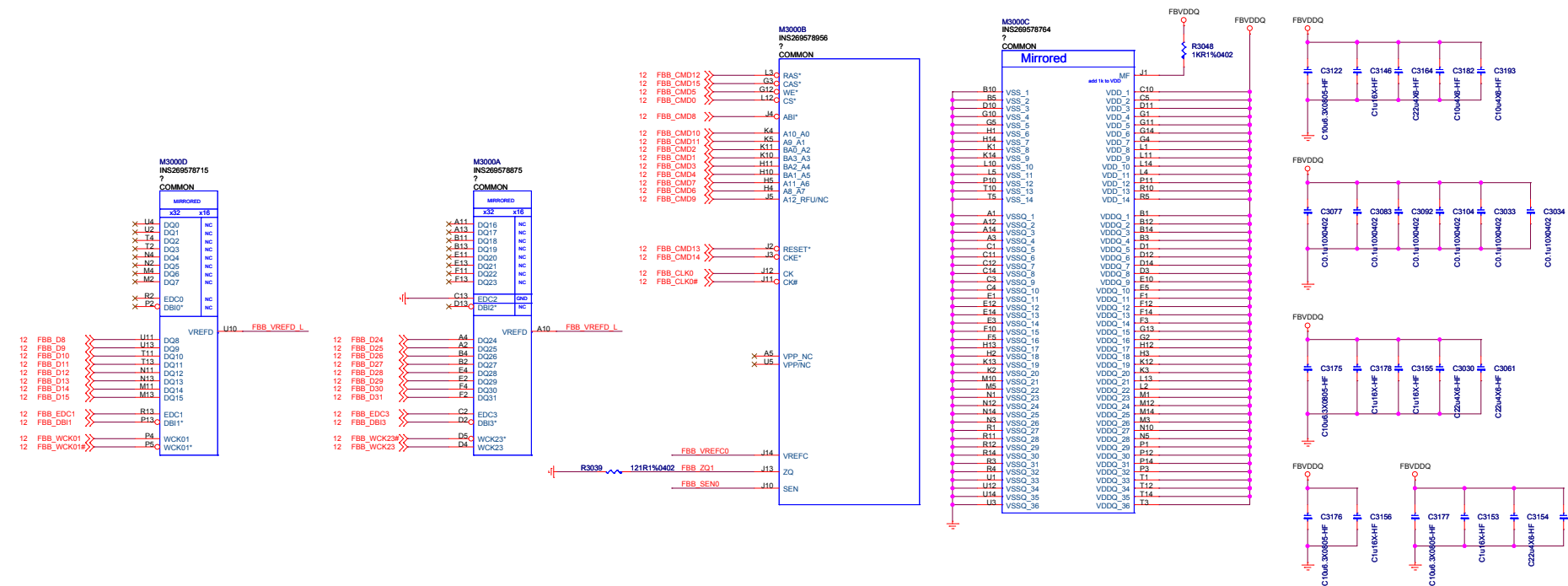
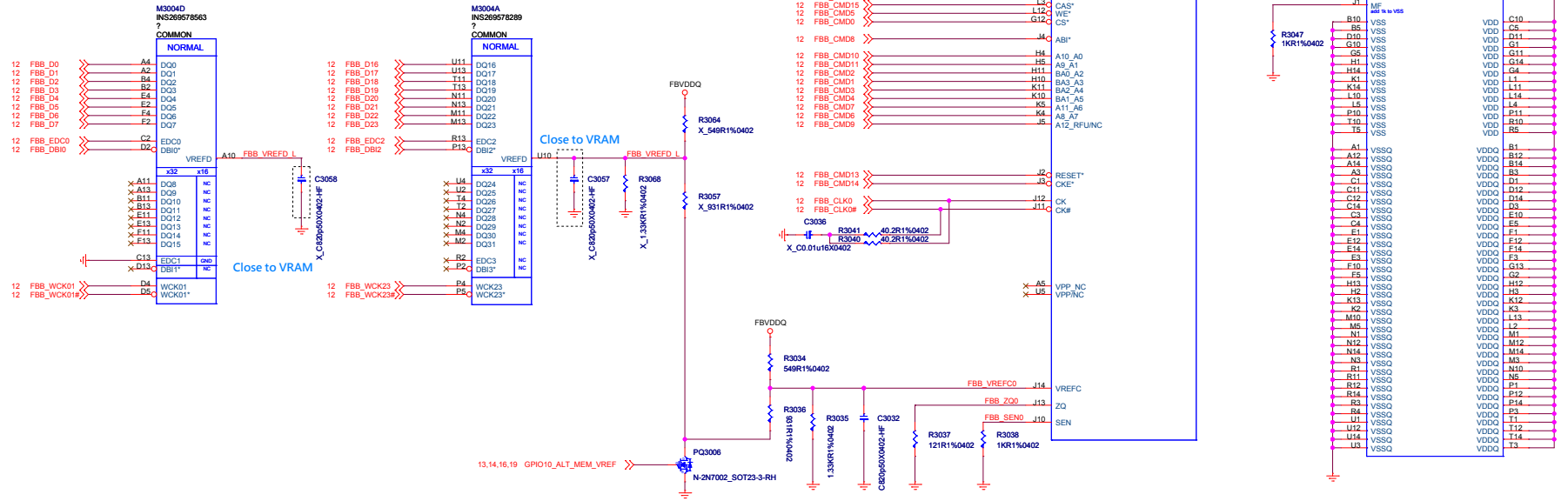


N16P-GX( GDDR5 Frame A-2 )



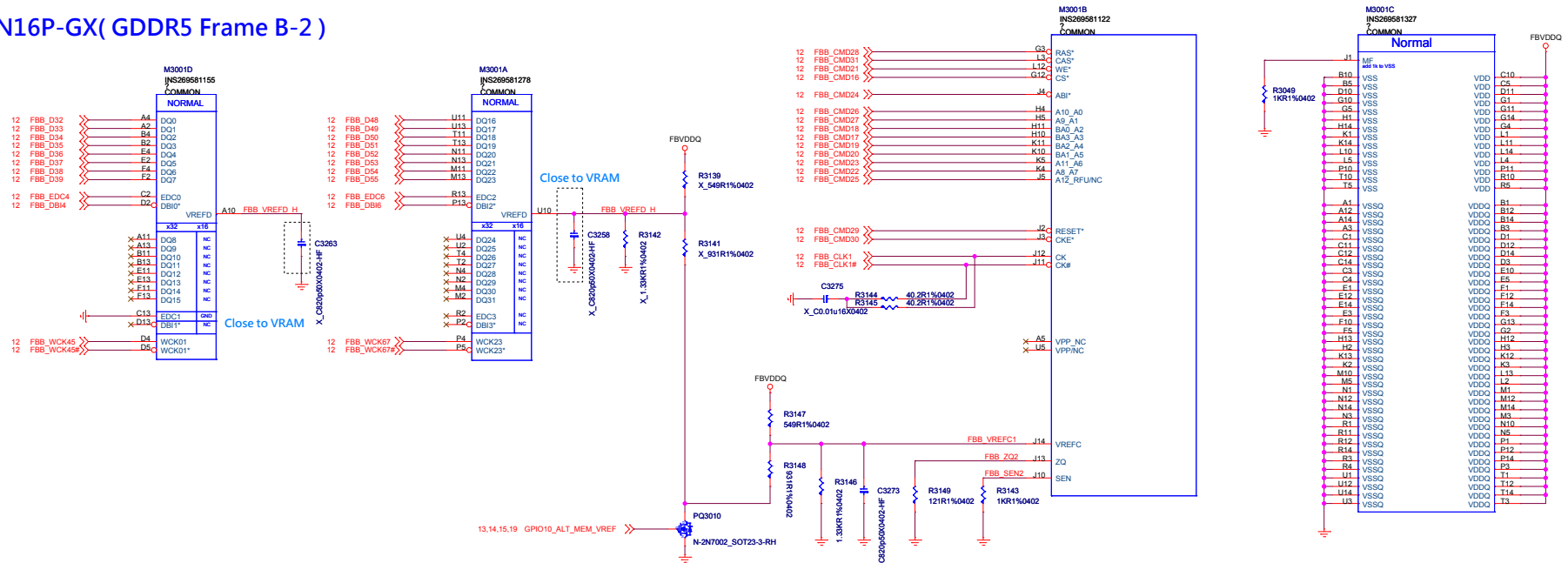


N16P-GX( GDDR5 Frame B-1 )



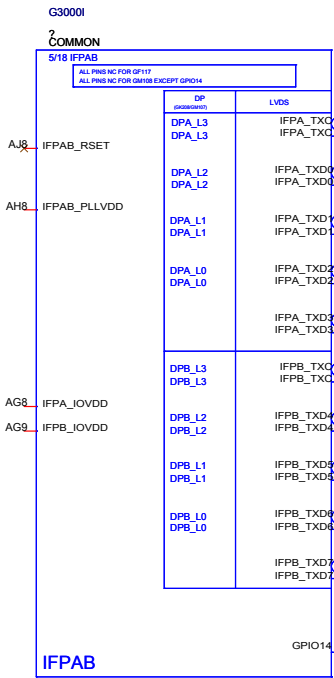


# N16P-GX( GDDR5 Frame B-2 )

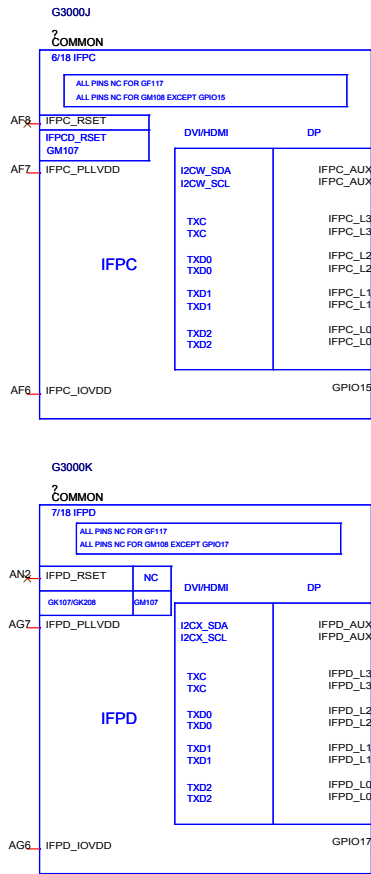


N16P-GX( Display IF)

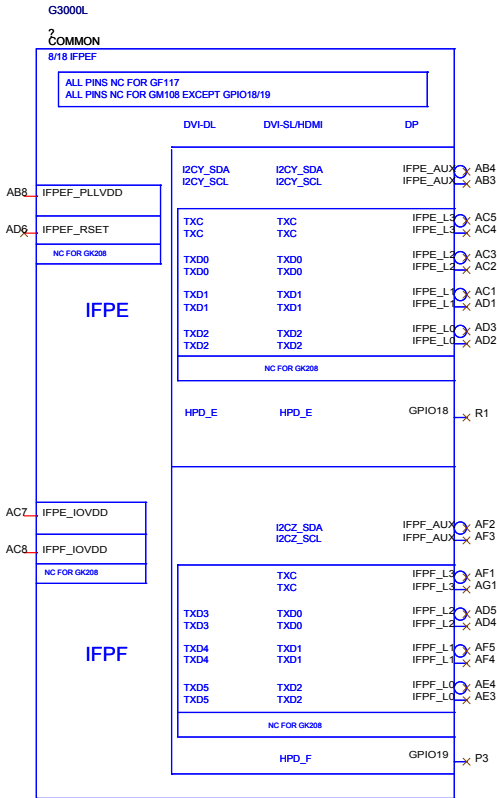
IFP A/B LVDSDual Link



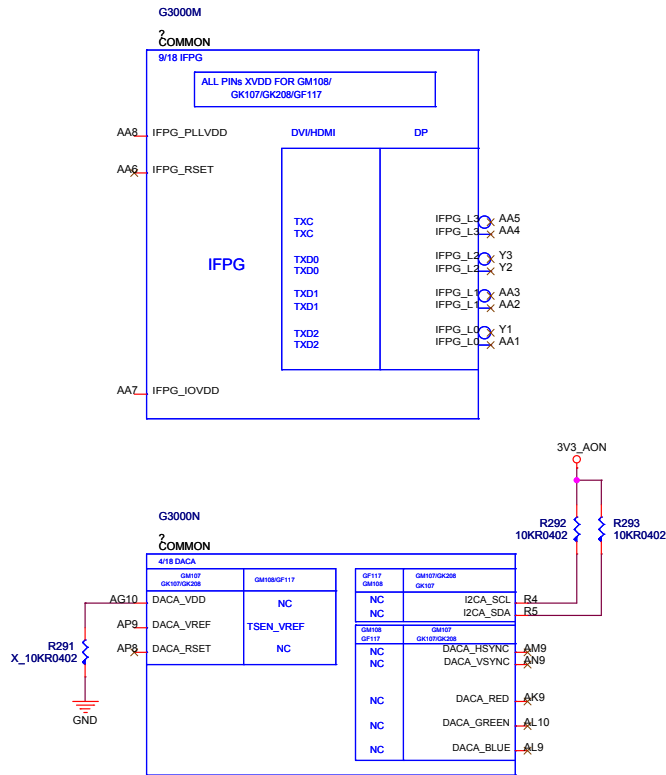
IFP C Native HDMI OR DP



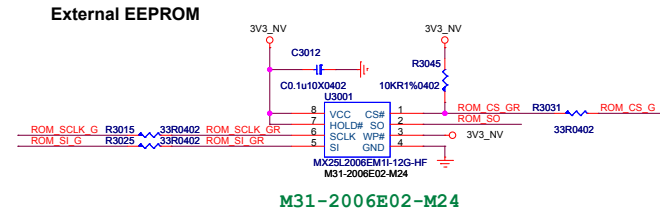
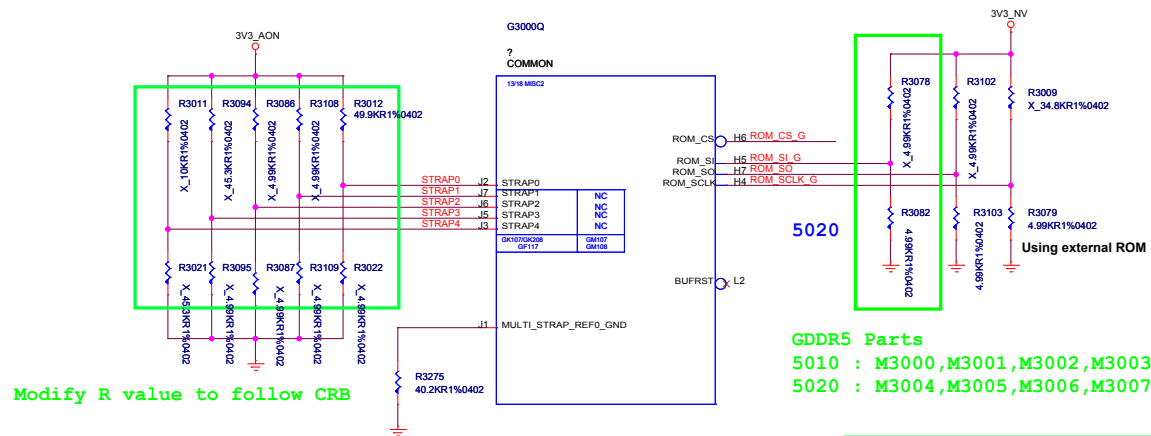
IFP E/F Dual Link TMDS DVI-I



DAC A VGA

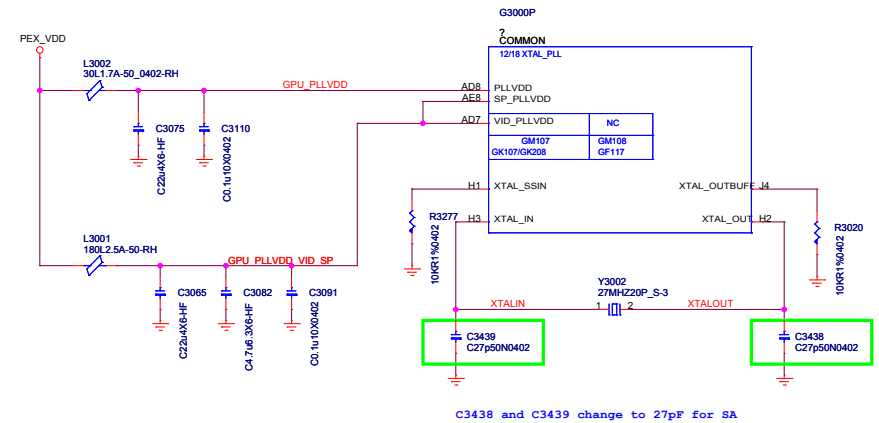


## ROM, MULTI-LEVEL STRAPS

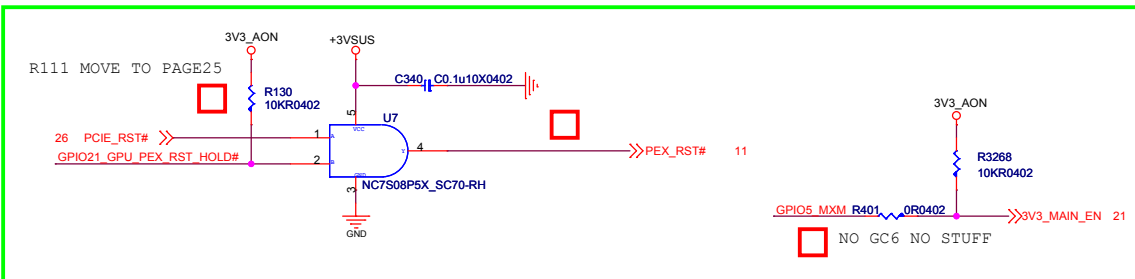
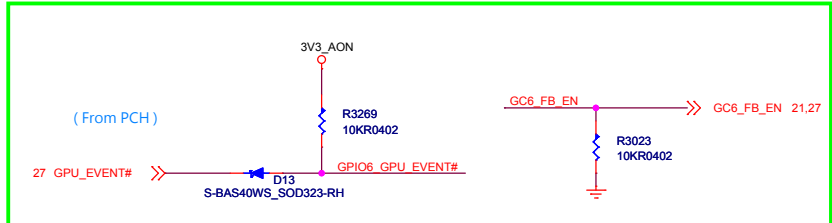
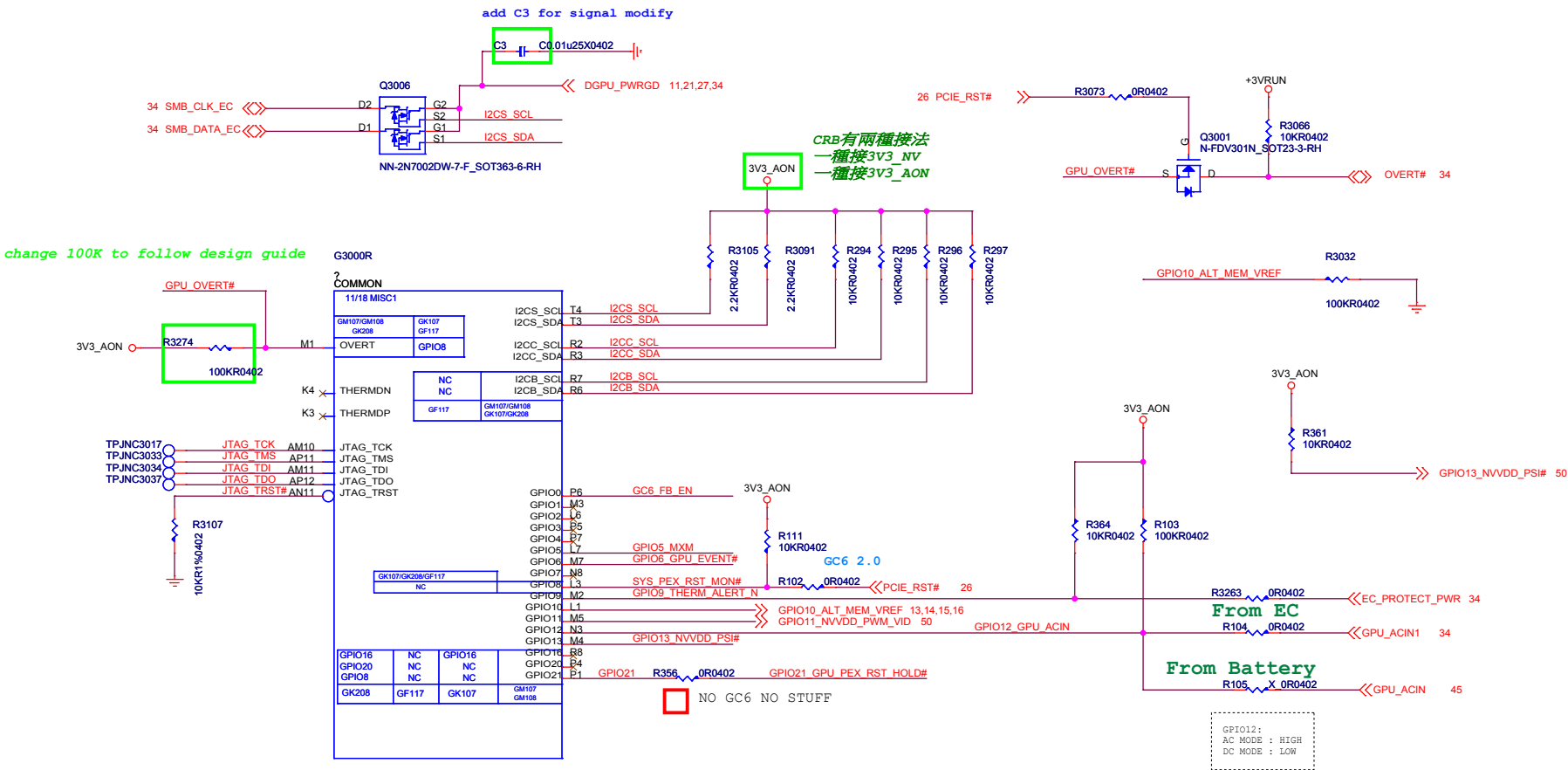


	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

ROM		Memory	
ROM_SI	RAM_CFG[3:0]	0x0 4.99K PD	Samsung 128x16bit
		0x1 10K PD	Hynix 128x16bit
		0x5 30.1K PD	Micron 128x16bit
ROM_SO	DEVID_SEL PCIE_CFG SMB_ALT_ADDR VGADEVICE	5K PD	
ROM_SCLK	SOR_EXposed[3:0]	5K PD	
STRAP0		50K PU 3V3_AON	
STRAP1		Reserved	
STRAP2		Reserved	
STRAP3		Reserved	
STRAP4		Reserved	

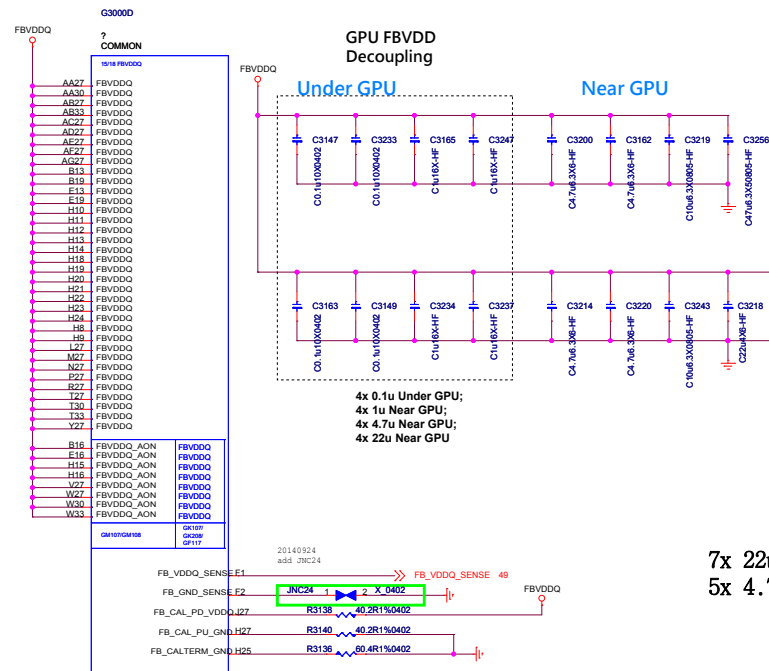


DEFAULT SETTING		BOT 記得轉階層	
ROM_S1	Samsung	V_TOP1	V_BOT1
 128Mx16bit		 5010	 5020
R11-499T12-W08		M12-2032585-S02	M12-2032585-S02
X_4.99KR1%0402		X_K4G20325FD-FC03	X_K4G20325FD-FC03
ROM_H1	Hynix	V_TOP2	V_BOT2
 128Mx16bit		 5010	 5020
R11-0103T12-W08		M12-5GC2H05-H23	M12-5GC2H05-H23
X_10KR1%0402		X_H5GC2H24BFR-T2C-HF	X_H5GC2H24BFR-T2C-HF
ROM_M1	Micron	V_TOP3	V_BOT3
 128Mx16bit		 5010	 5020
R11-3012T12-W08		M12-2032B95-M30	M12-2032B95-M30
X_30.1KR1%0402		X_EDW2032BBBG-6A-F	X_EDW2032BBBG-6A-F

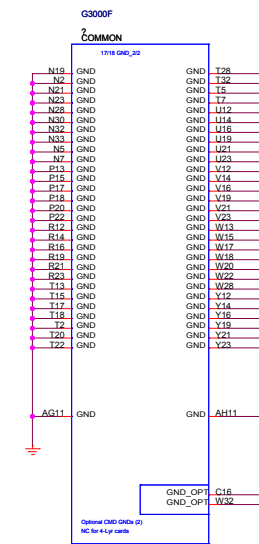
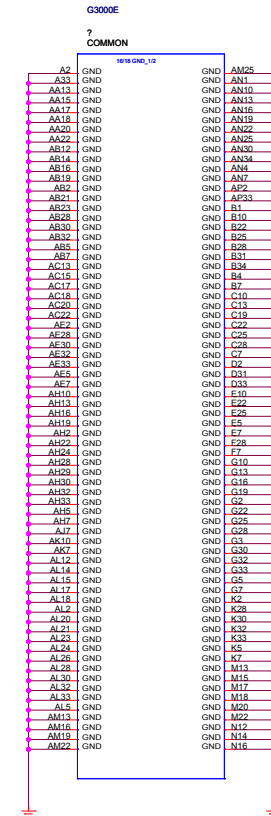
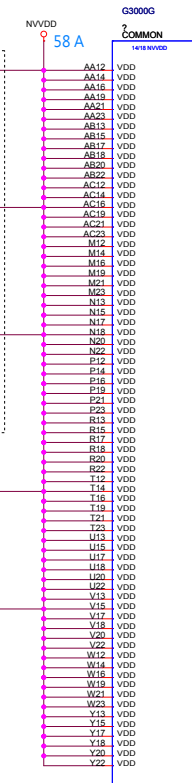
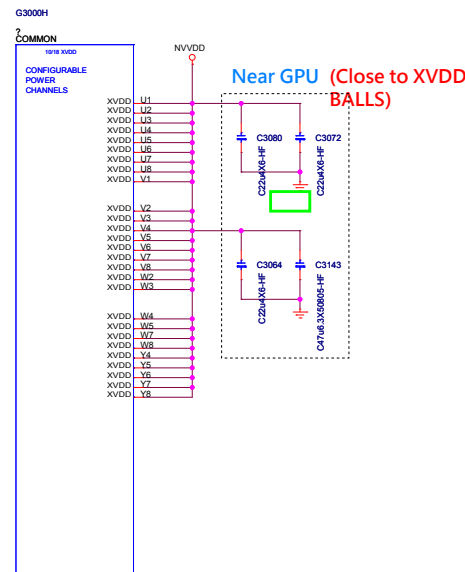


## N16P-GX( Power & GND )

8x 1u Under GPU;  
15x 4.7u Under GPU

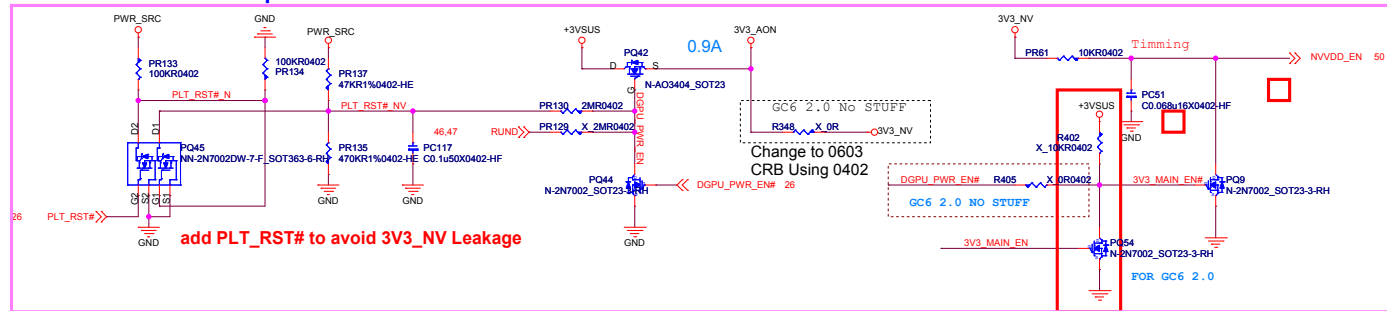


7x 22u near GPU  
5x 4.7u near GPU

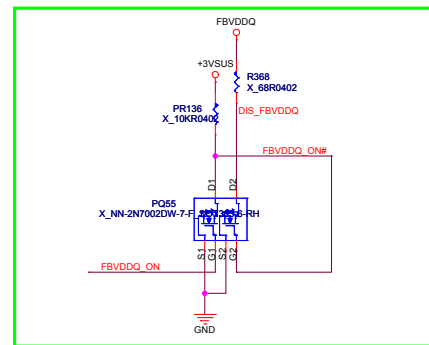
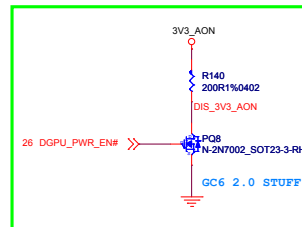
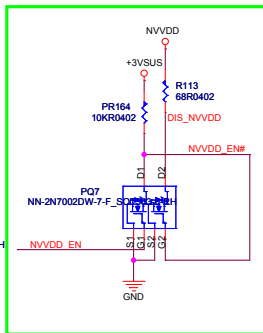
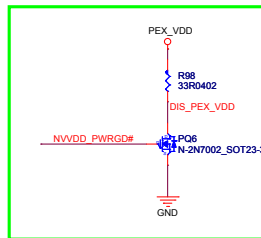


## N16P-GX( Power Control )

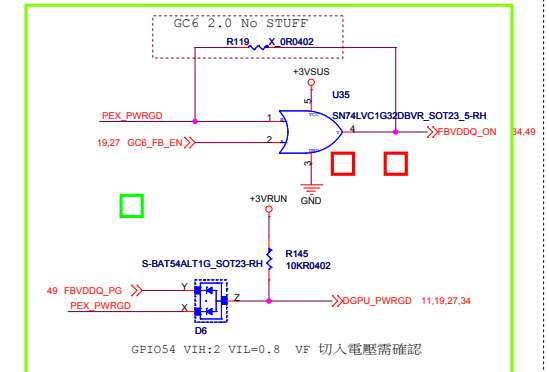
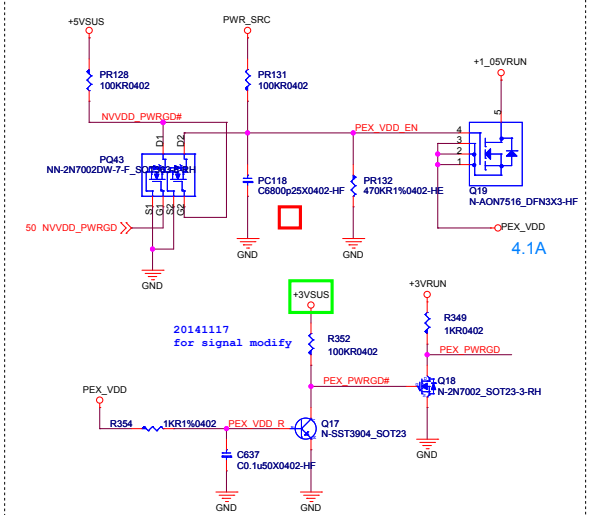
nVIDIA Power Sequence Control 3V3\_AON -> 3V3\_NV -> NVVDD -> PEX\_VDD -> FBVDDQ -> DGPUPWRGD



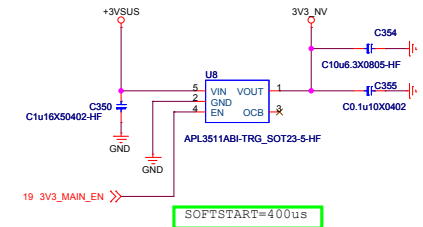
## Discharge Circuit



## PEX\_VDD



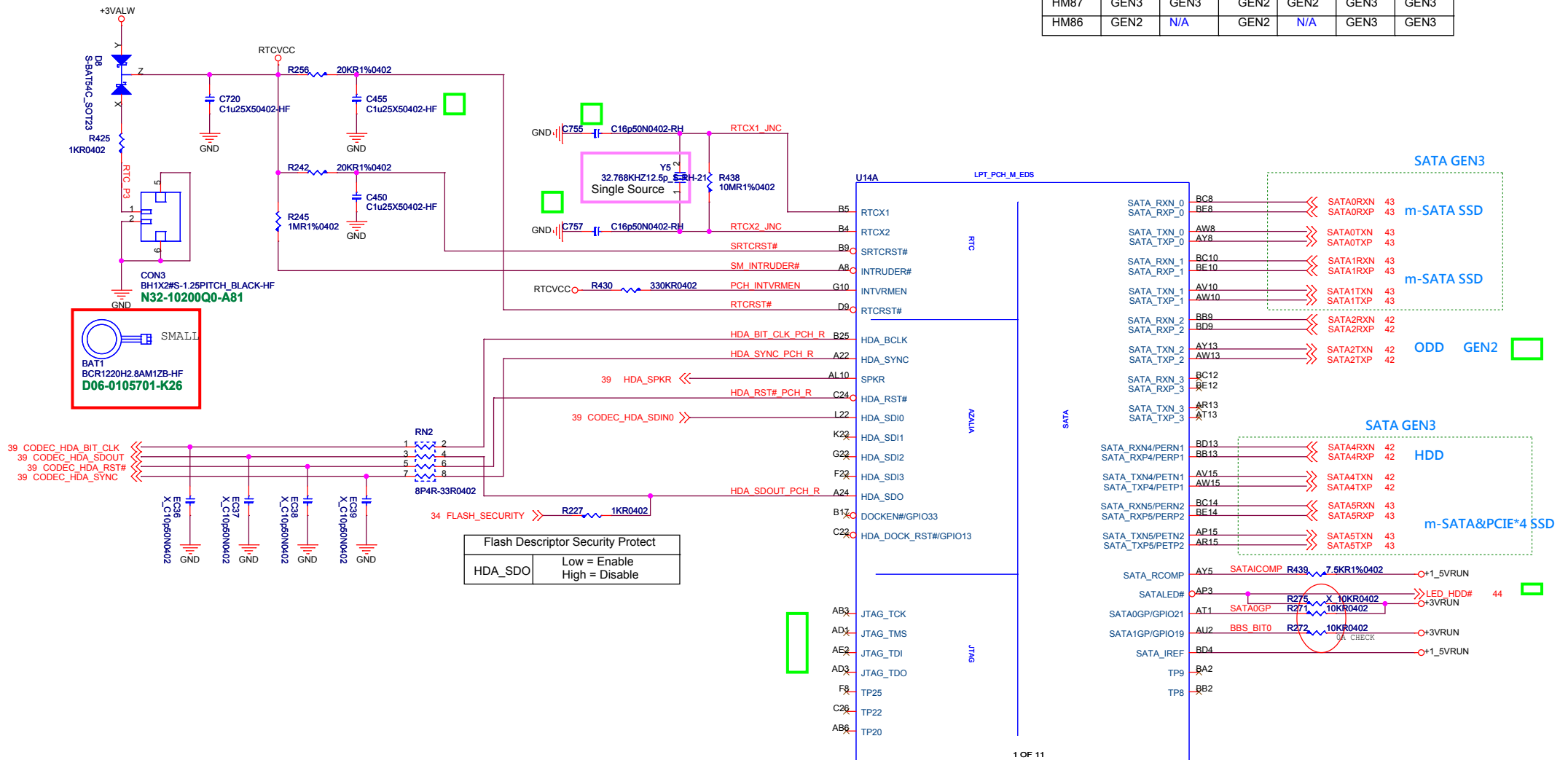
## GC6 2.0 STUFF



Title			
N16P-GX Power Control			
Size	Document Number	Rev	
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Date:	Thursday, November 27, 2014	Sheet	21 of 59

# Lynx Point ( HDA/JTAG/SATA )

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3

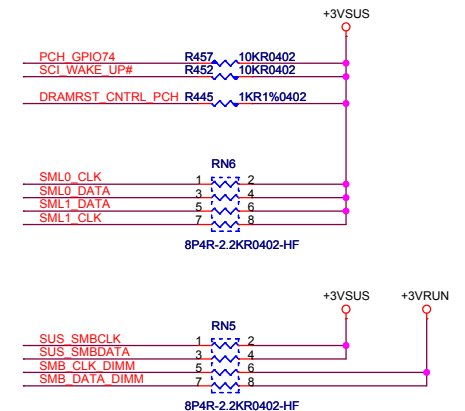
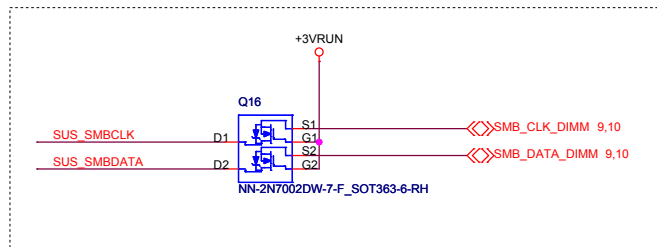
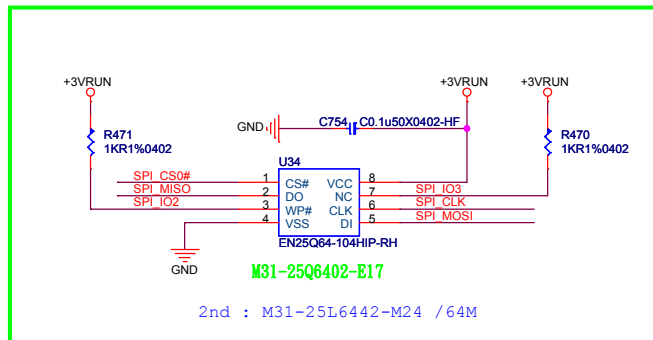
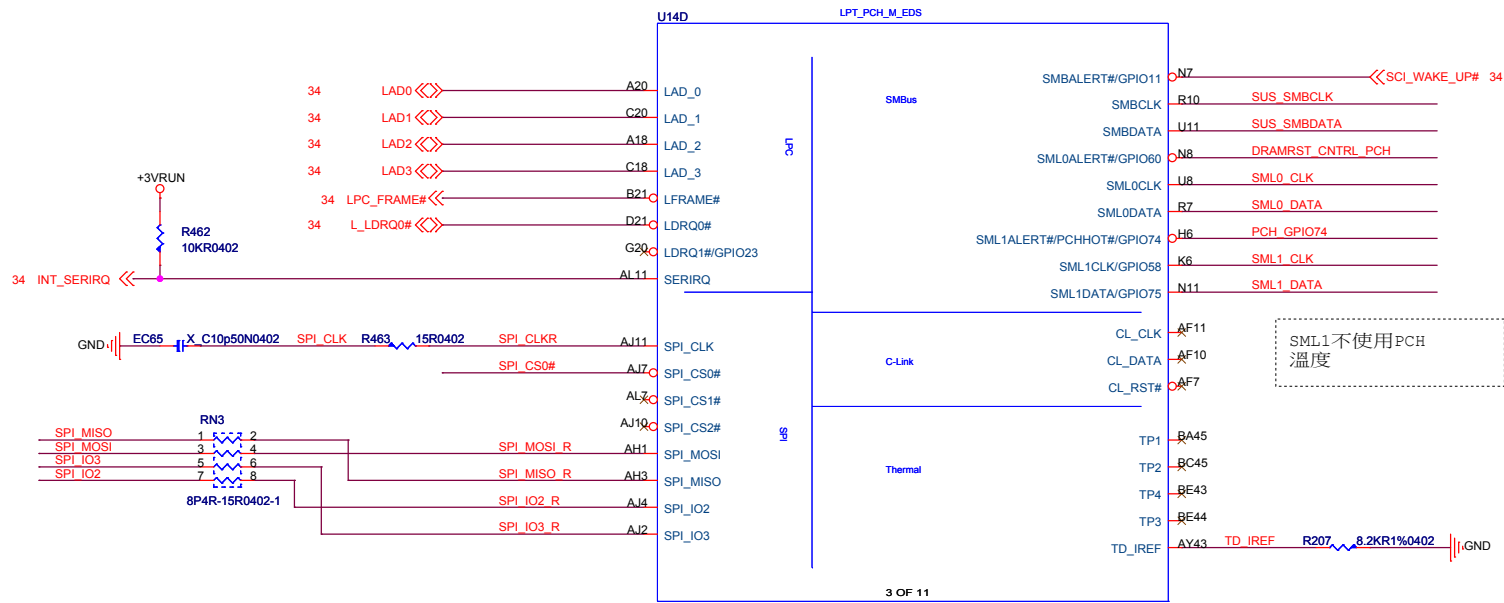


SPK The Signal has a weak internal pull-down  
Note: the internal pull-down is disabled after PLTRST# deasserts.  
If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode  
(Panther Point will disable the TCO Timer system reboot feature)

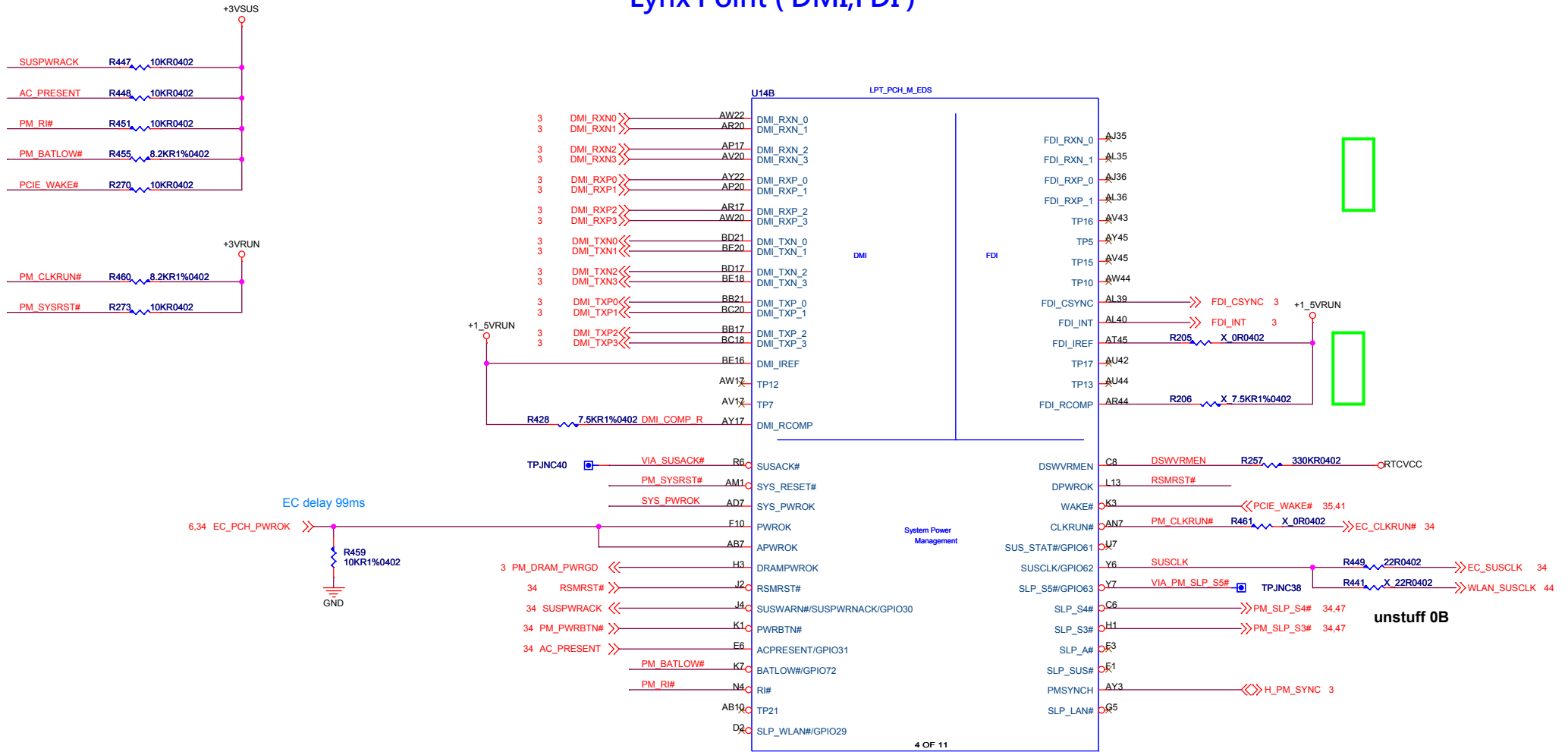




# Lynx Point ( LPC,SMBUS )



# Lynx Point ( DMI,FDI )



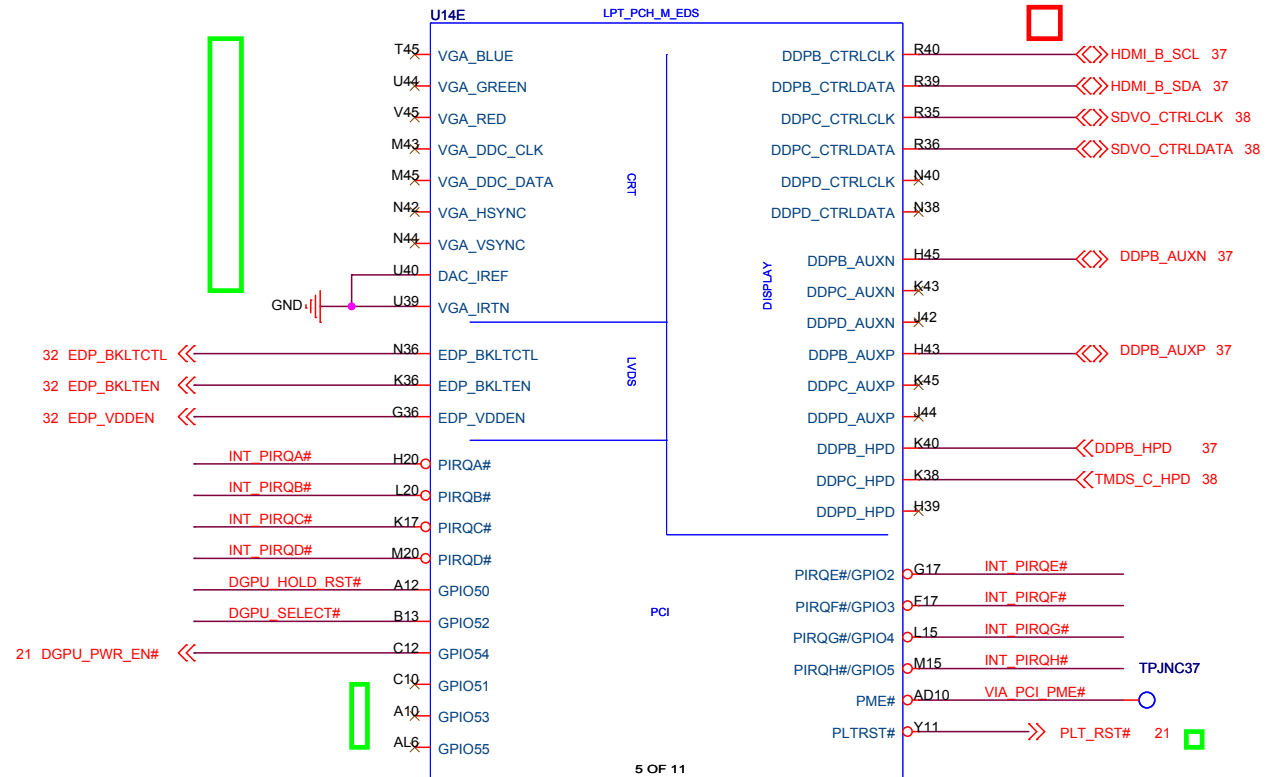
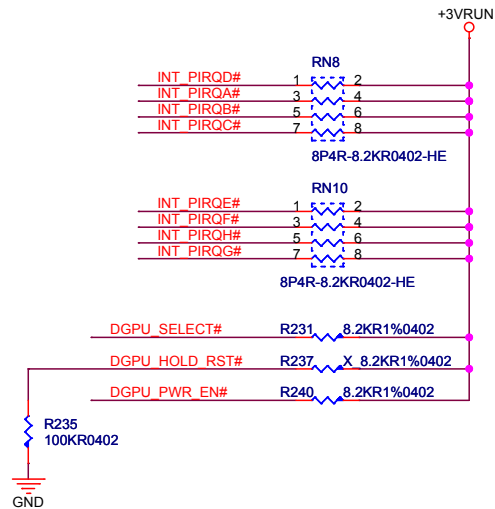
APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWMRST# - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708\_LPT\_EDS Section2.18

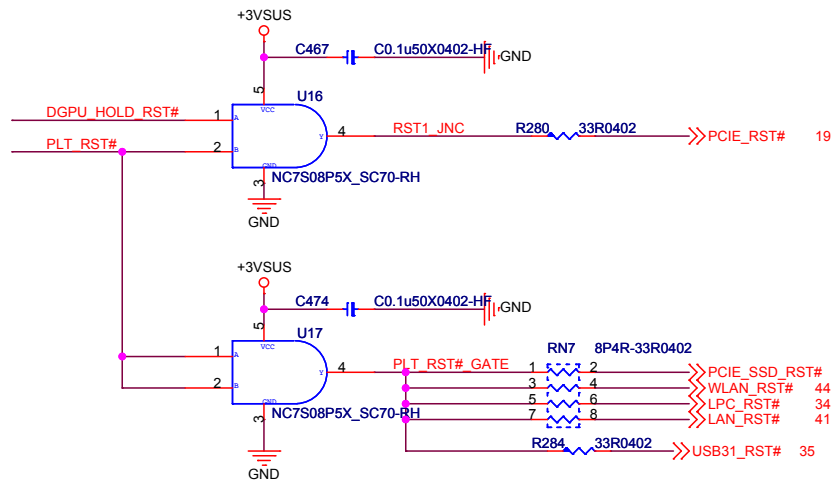
PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

# Lynx Point ( PCI,DDI )

CTRLDATA This signal needs to be pulled up through a 2.2 kOhms  $\pm 5\%$  pull-up to 3.3 V to " enable Port" .



DDI-B : DP  
DDI-C : HDMI

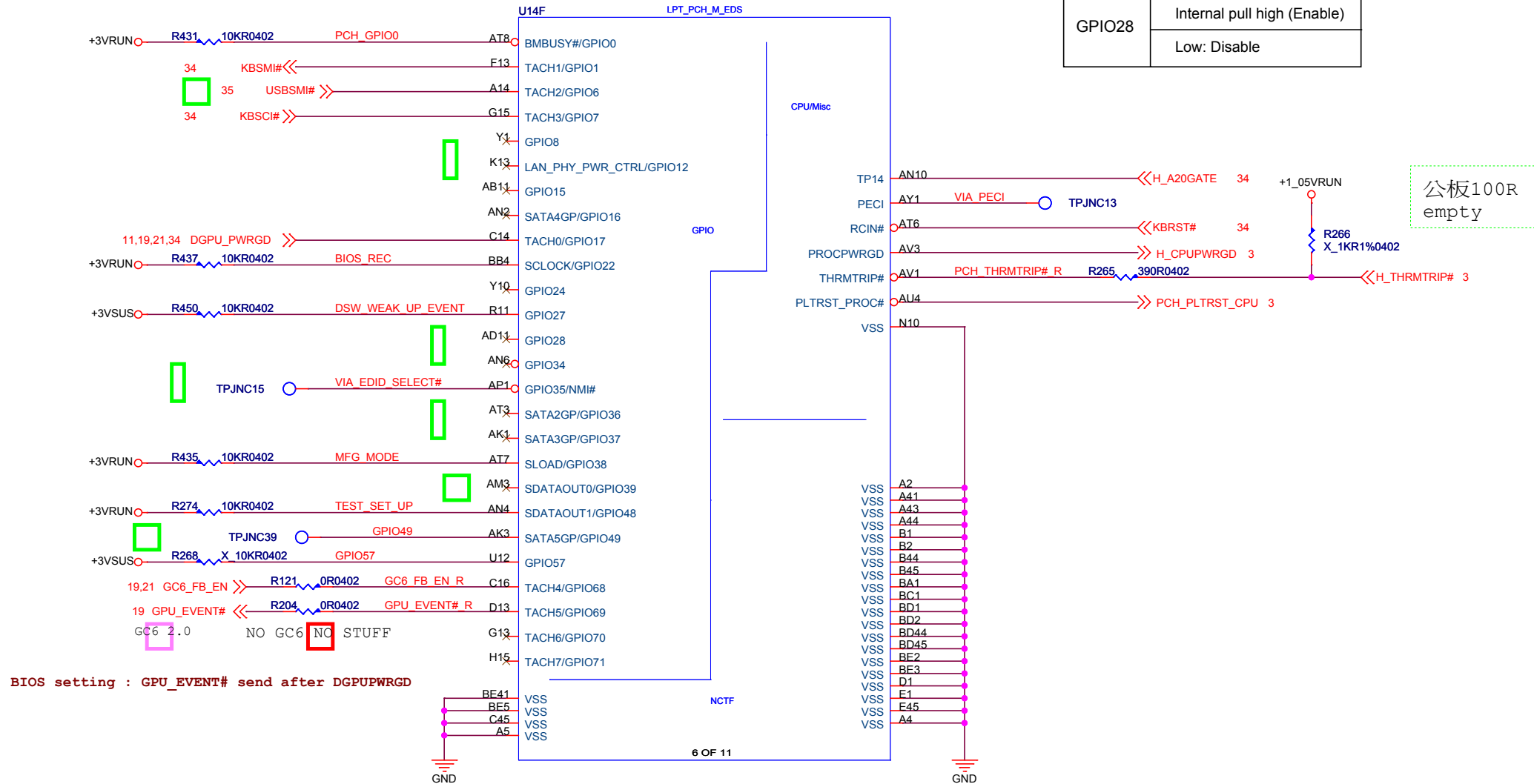


Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

## Lynx Point ( GPIO,MISC )

**GPIO Setting : Ref 486708\_LPT\_EDS Section2.24**

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



# Lynx Point ( PCIE,USB )

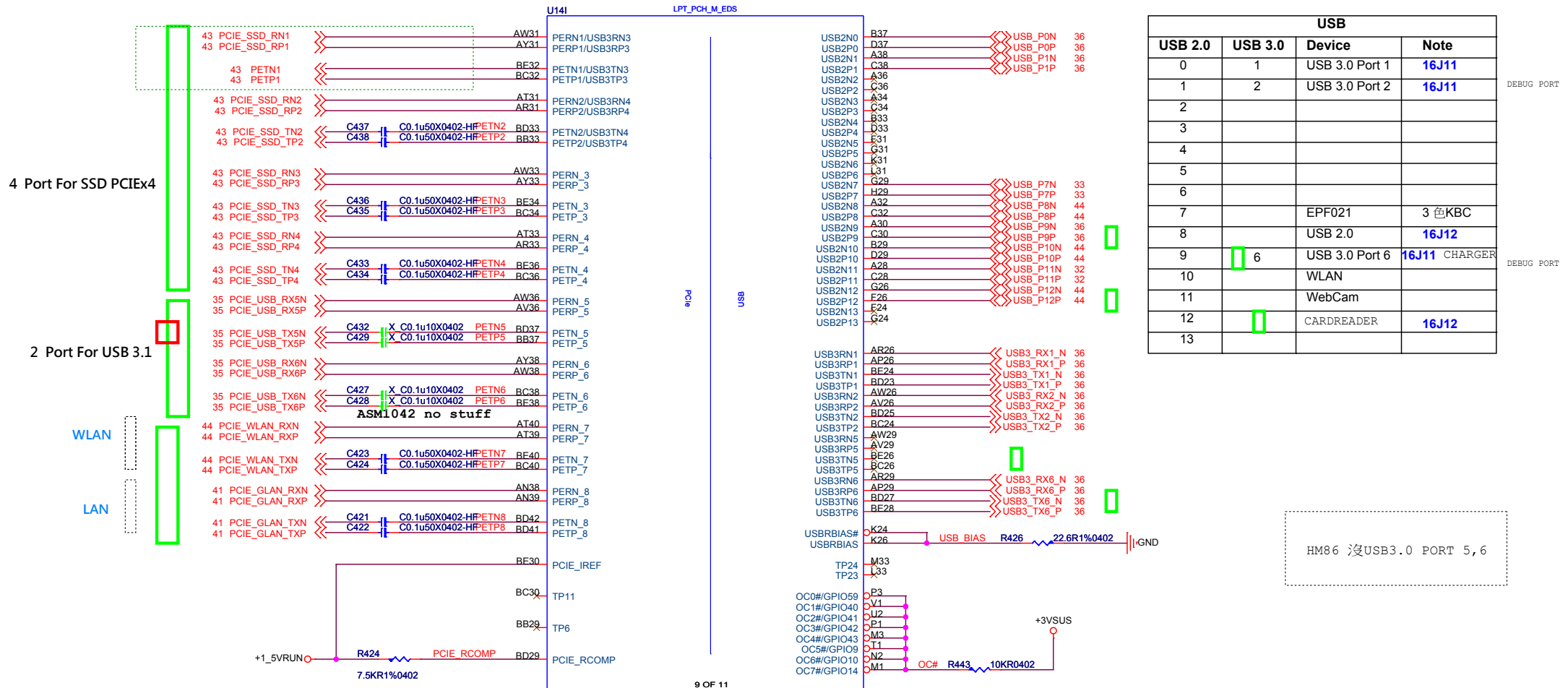
Table 5-1. PCI Express\* Ports 1 thru 4 - Supported Configurations

Port 1	Port 2	Port 3	Port 4
x4			
x2		x2	
x2		x1	x1
x1	x1	x1	x1

Table 5-2. PCI Express\* Ports 5 thru 8 - Supported Configurations

Port 5	Port 6	Port 7	Port 8
x4			
x2		x2	
x2		x1	x1
x1	x1	x1	x1

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9



**Lynx Point ( Power )**

The diagram illustrates the power distribution network for the Lynx Point, showing the +1\_05VRUN and +1\_5VRUN rails, their decoupling capacitors, and the power requirements of various components.

**Power Requirements (mA):**

- +1\_05VRUN: 1.312A (Total), 670 mA (Decoupling)
- +1\_5VRUN: 3.629A (Total), 183 mA (Decoupling)
- Other components: 70 mA, 98 mA, 261 mA, 476 mA, 3.629 A

**Components and Connections:**

- Capacitors:** C732, C726, C727, C729, C714, C723, C695, C733, C734, C702, C701, C717, C735, C758, C721, C794.
- Resistors:** R427, R30, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100.
- Connectors:** TPJNC36, TPJNC31.
- Components:** U14G, U14, U14.AK18, U14.AK22, U14.AK20, U14.AM18, U14.AK18, U14.AN34.

**Legend:**

- Blue: Power Plane
- Red: Signal Plane
- Green: Ground Plane

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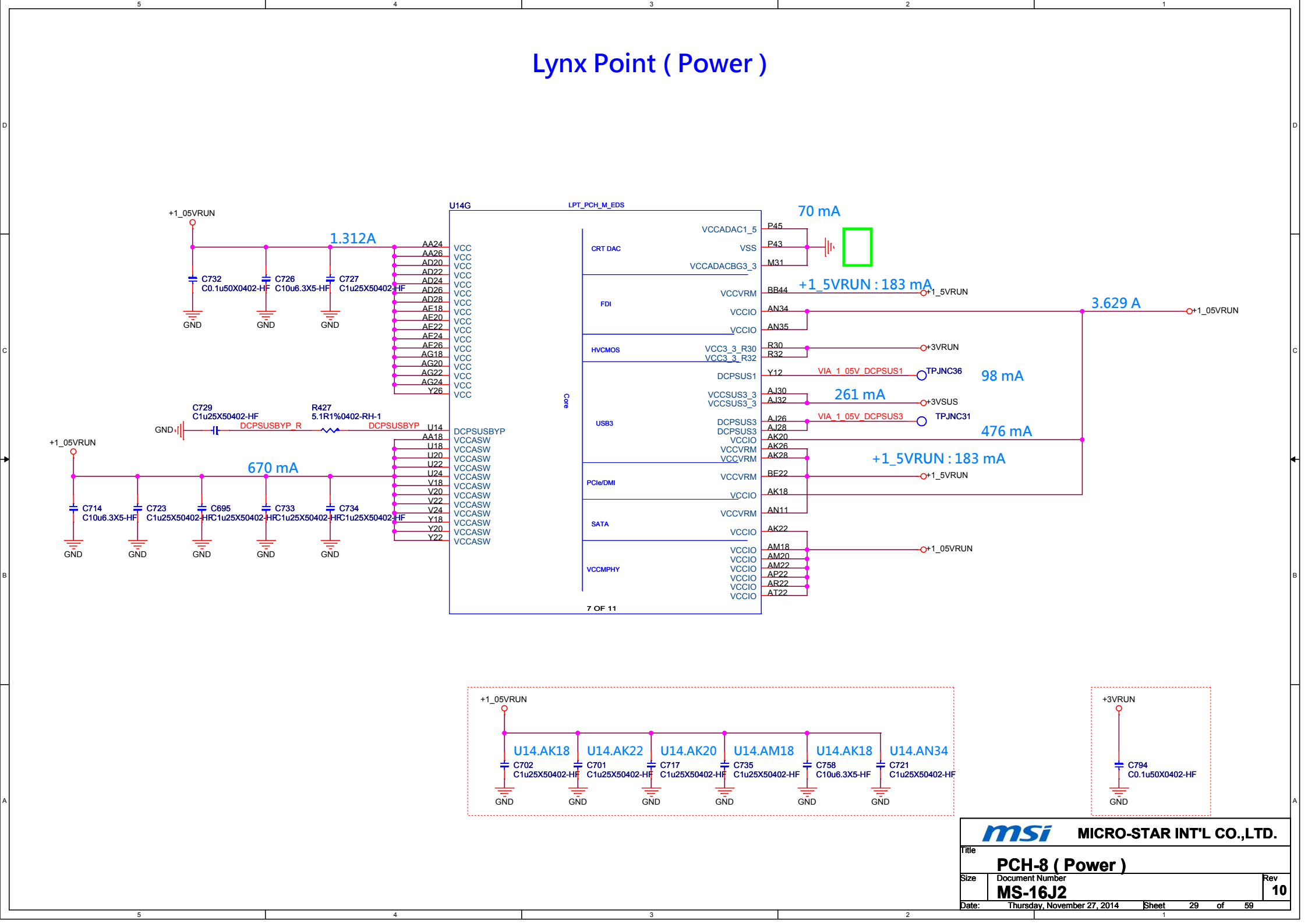
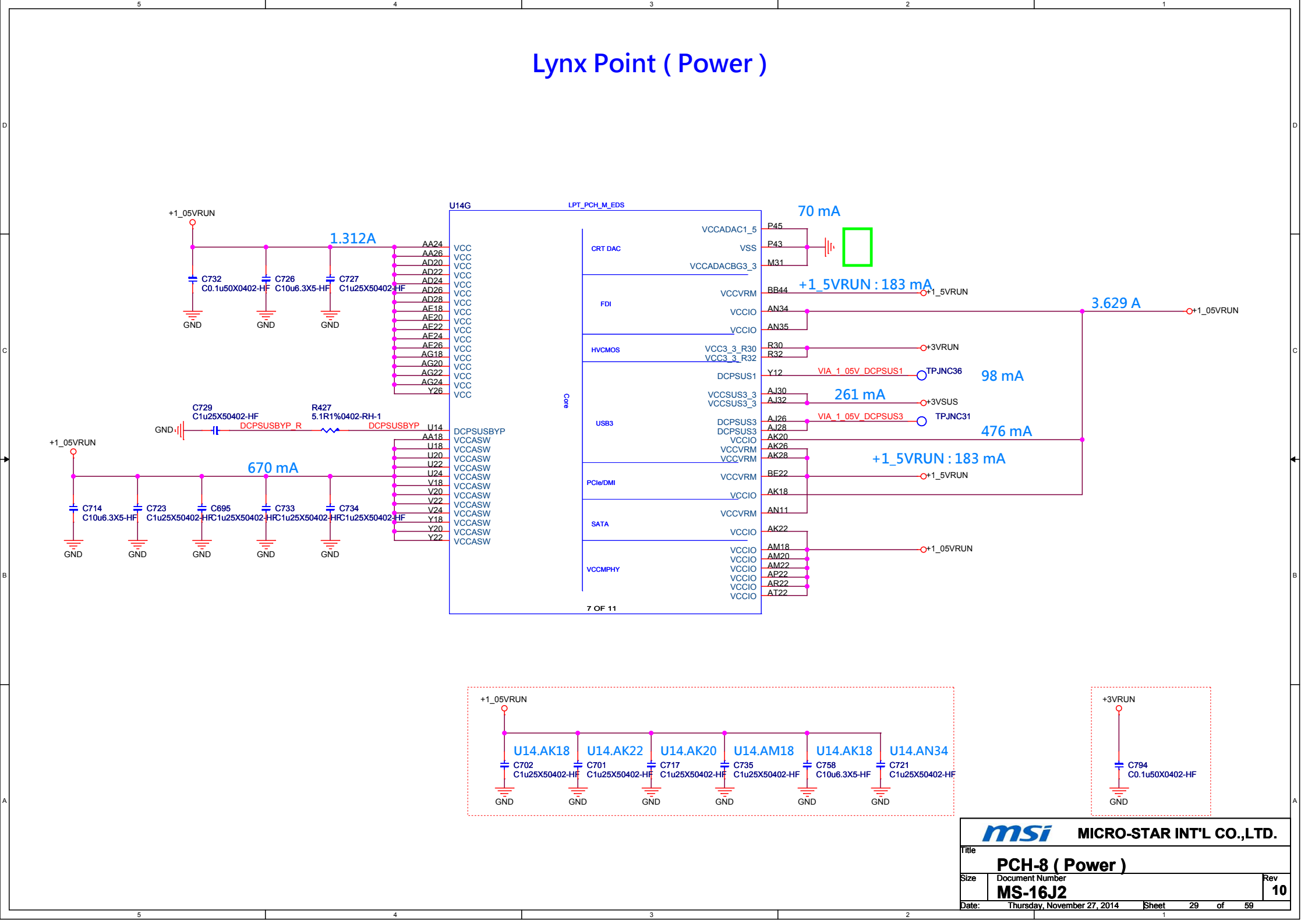
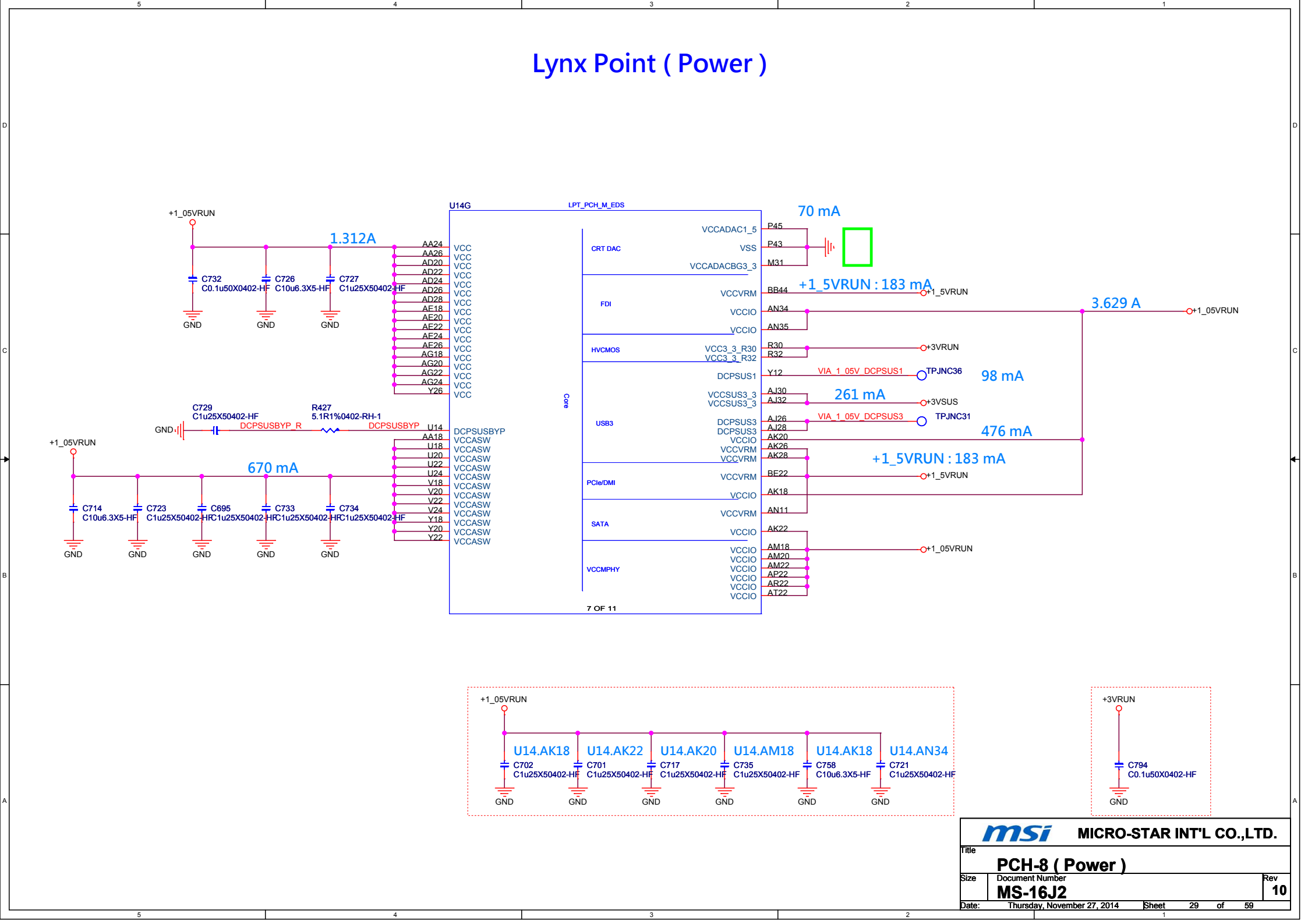
**Title:** PCH-8 ( Power )

**Size:** Document Number MS-16J2

**Date:** Thursday, November 27, 2014

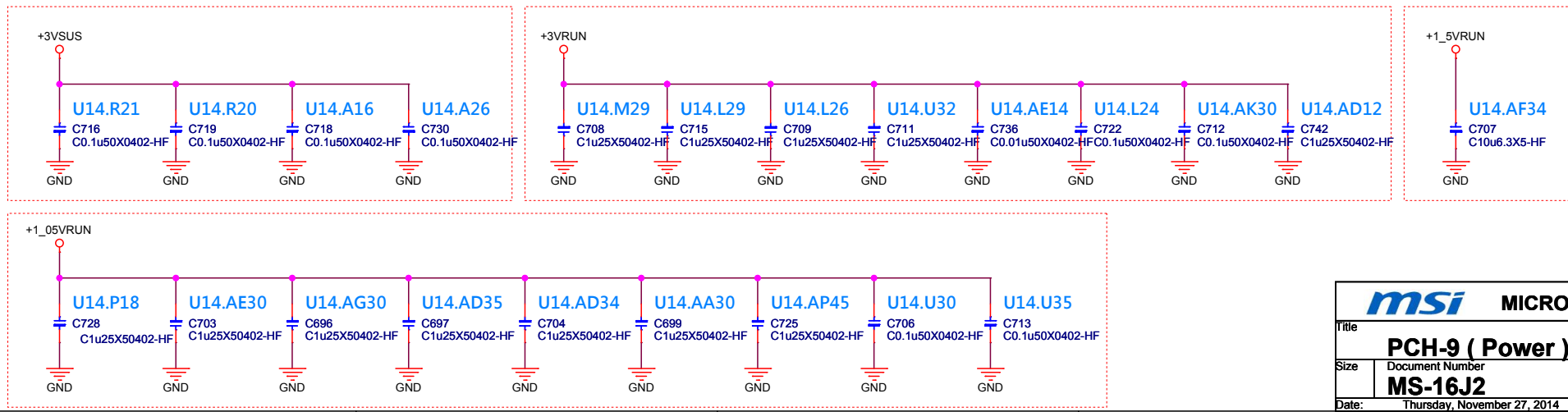
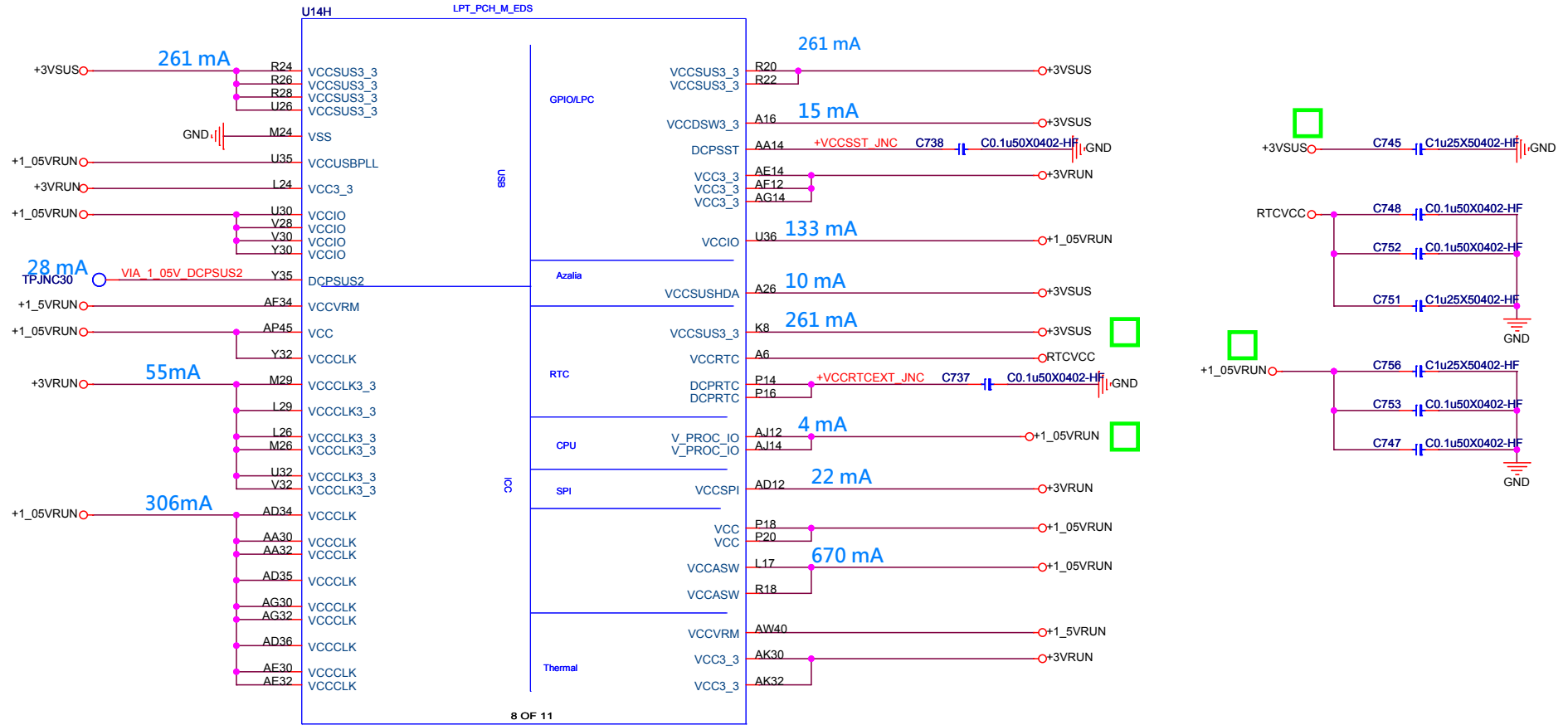
**Sheet:** 29 of 59

**Rev:** 10

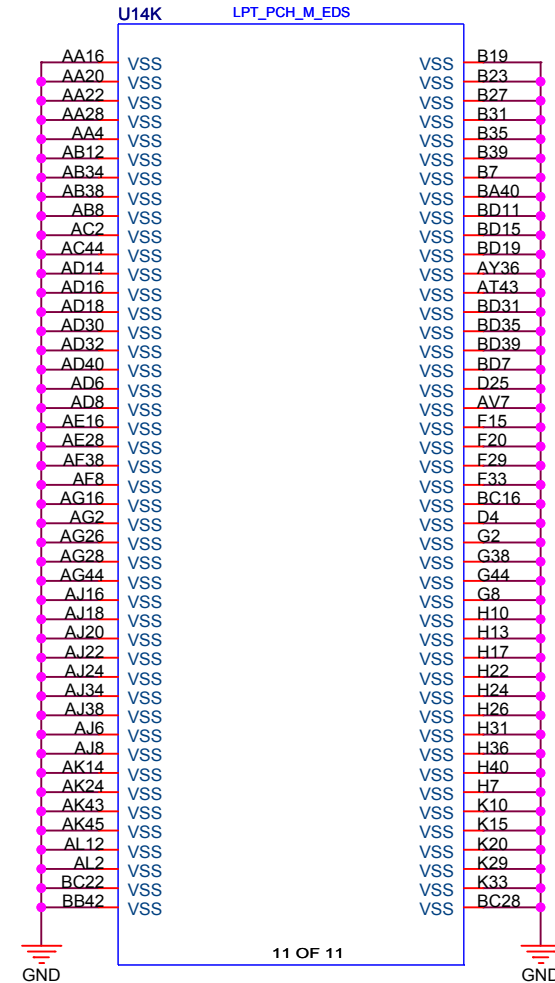
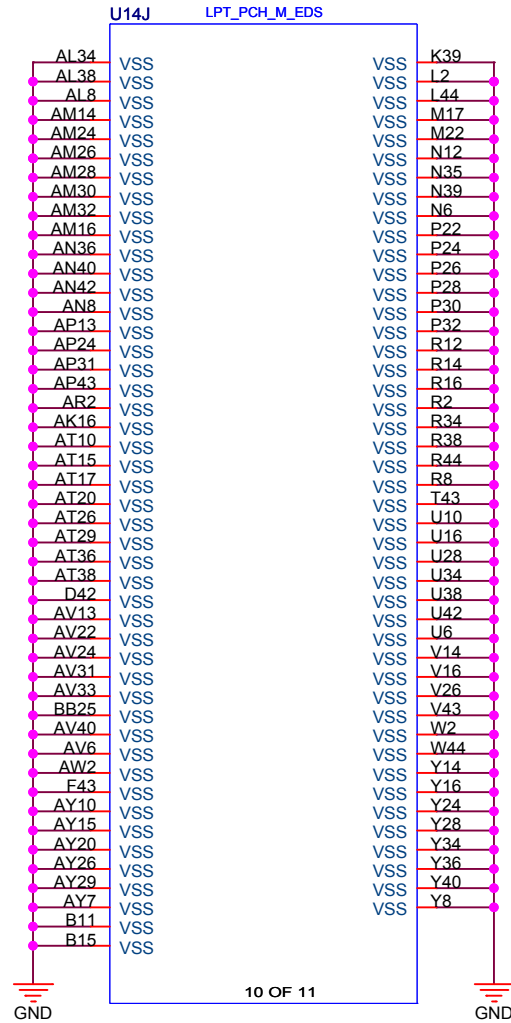




# Lynx Point ( Power )



# Lynx Point ( GND )

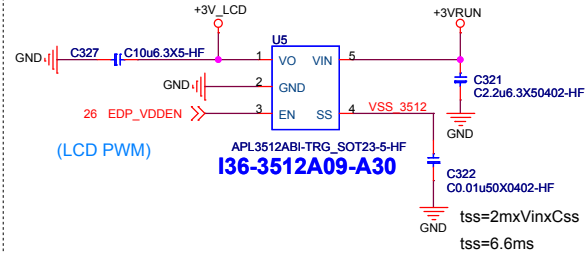


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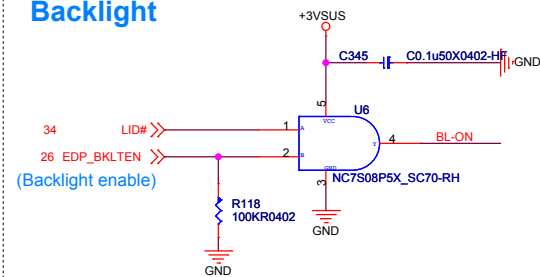
Title					<b>PCH-10 ( GND )</b>					
Size		Document Number					Rev		<b>10</b>	
		<b>MS-16J2</b>								
Date:		Thursday, November 27, 2014			Sheet		31		of 59	

## eDP

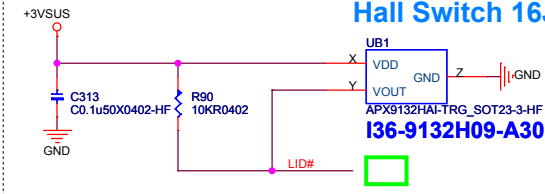
### Pannel Device Logic Power



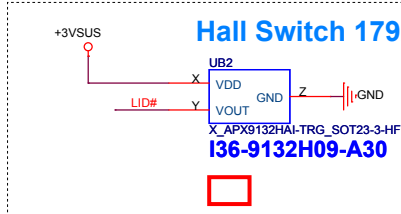
### Backlight



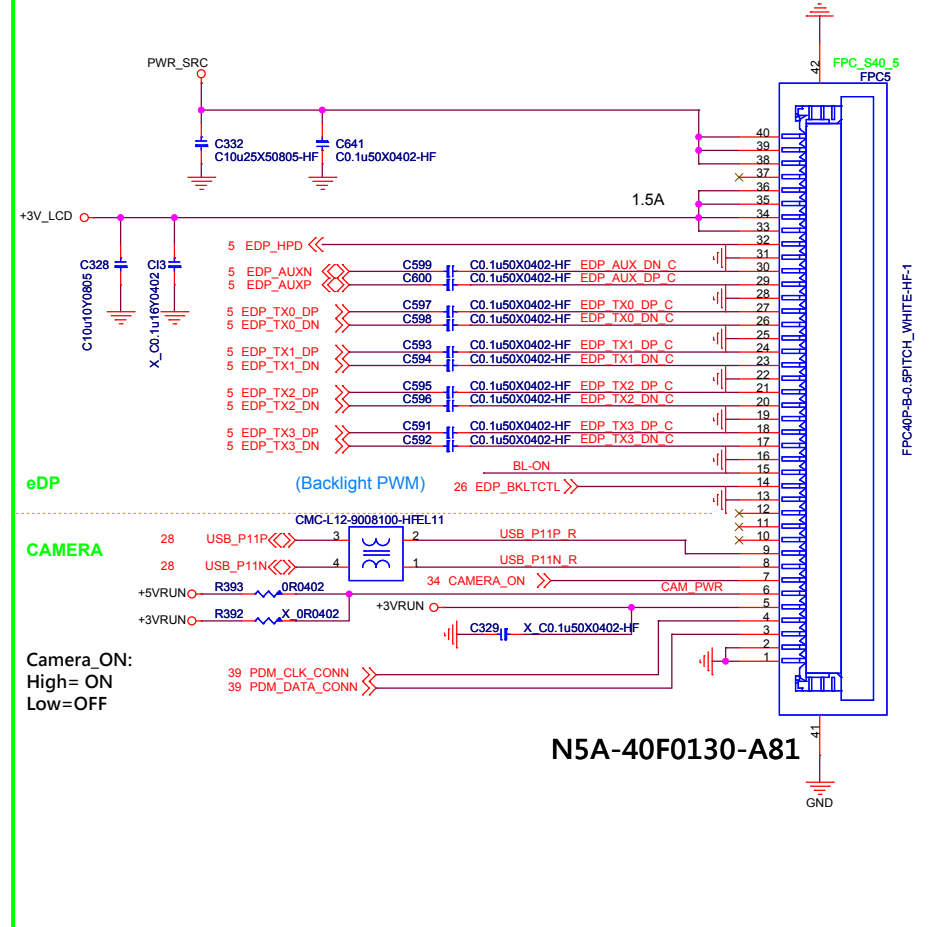
### Hall Switch 16J2



### Hall Switch 1792

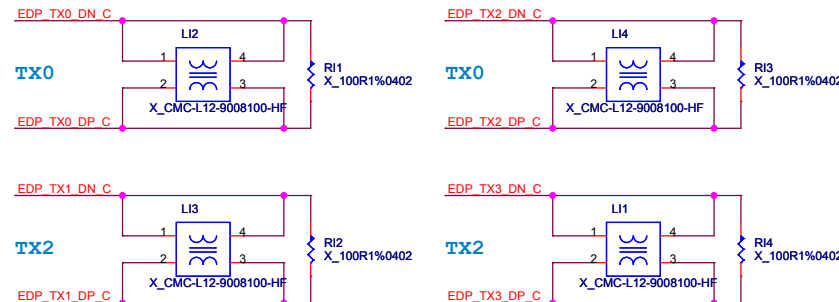


## eDP CONN CAMERA



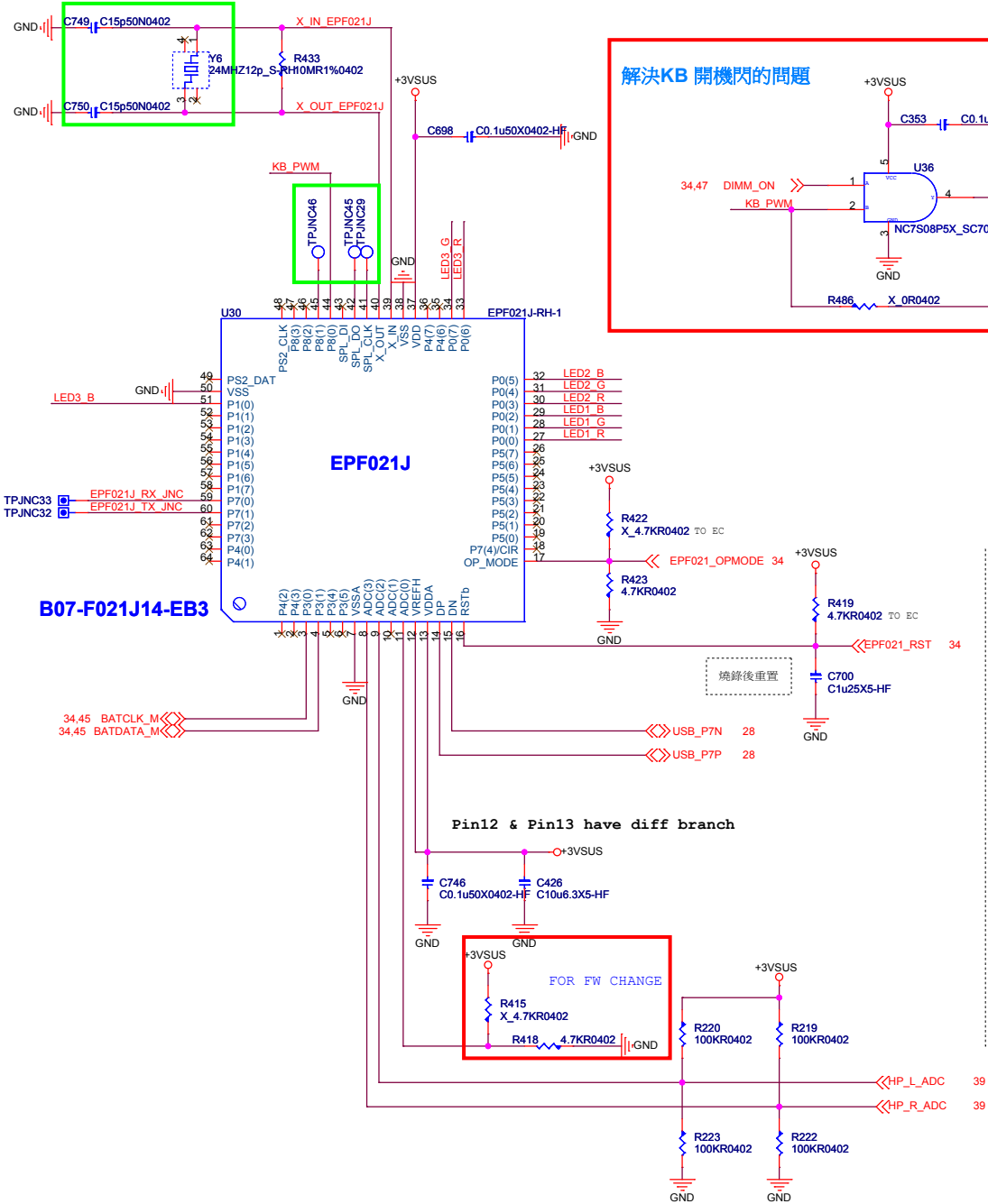
## LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

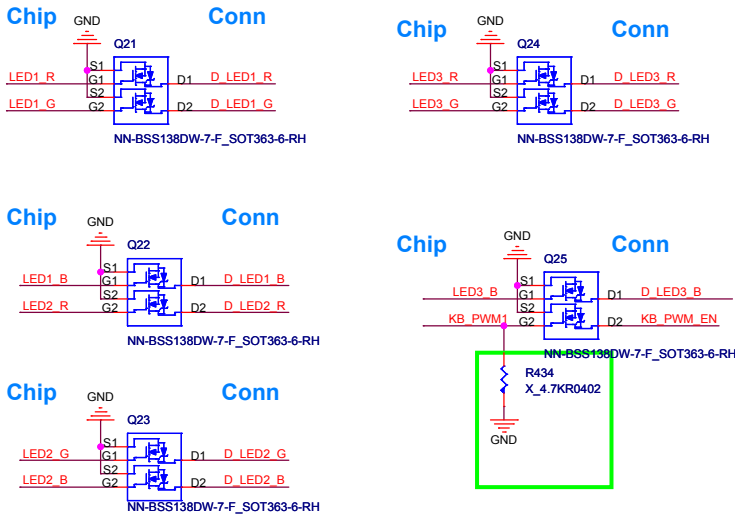


LED 8051 Controller

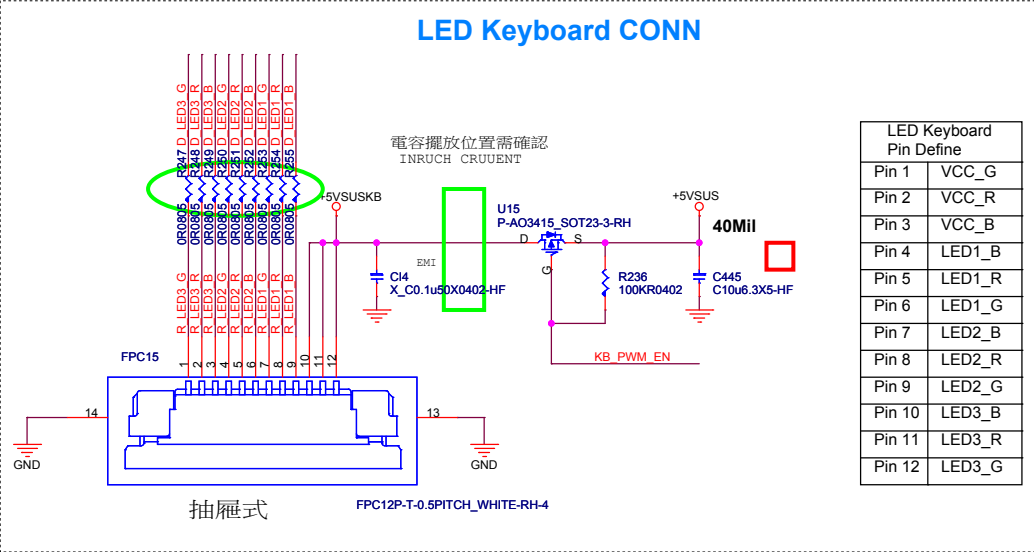
C749 and C750 change to 15pF for SA



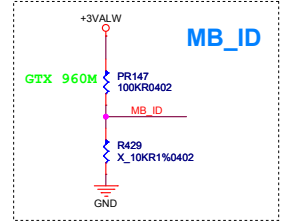
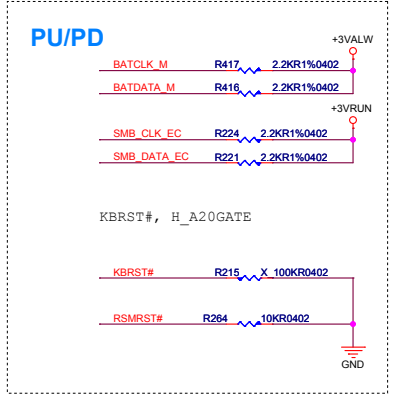
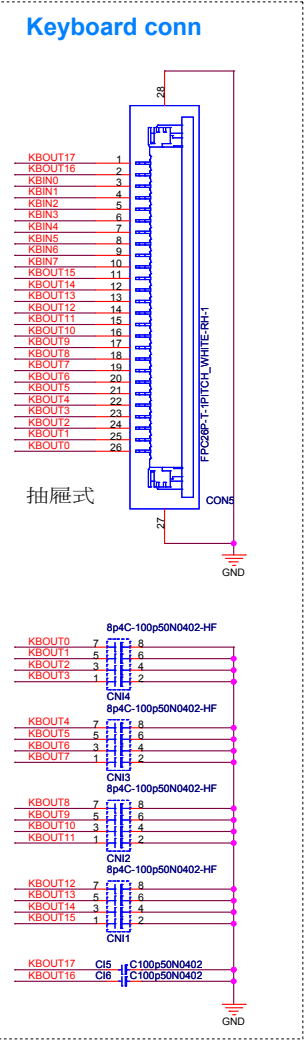
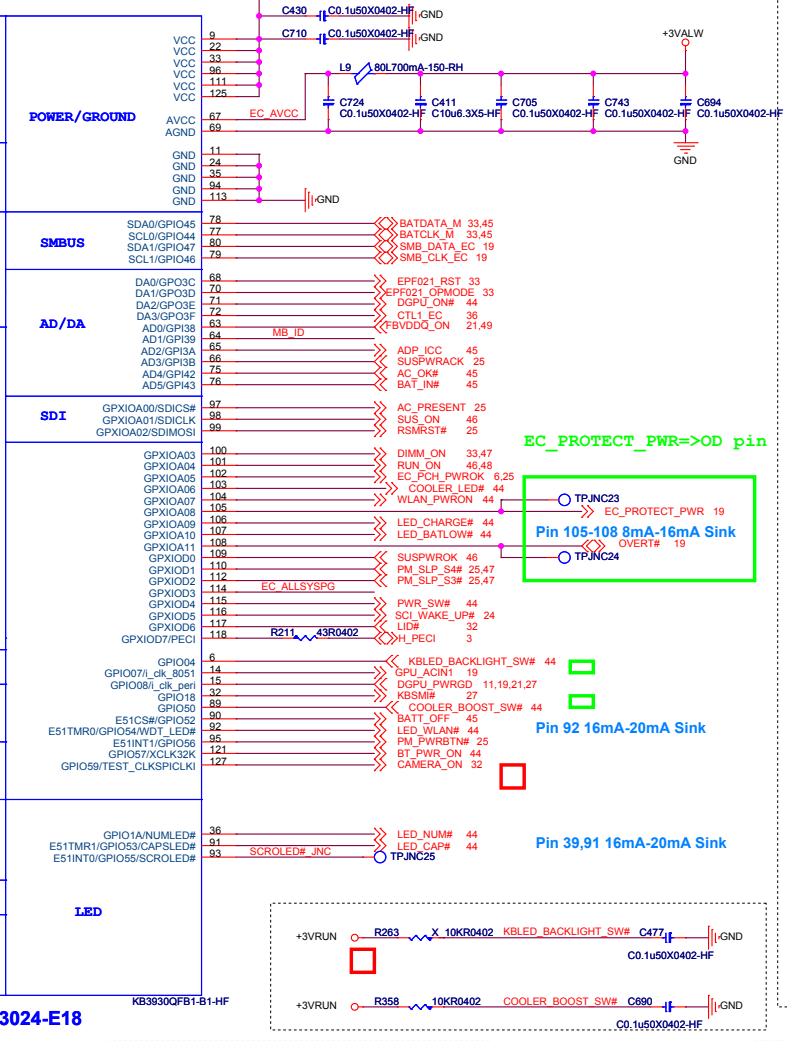
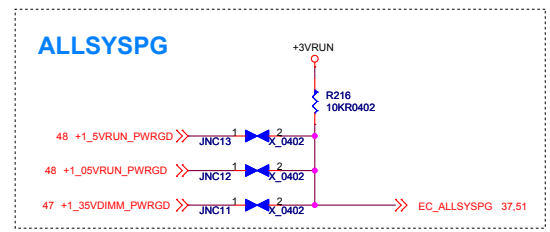
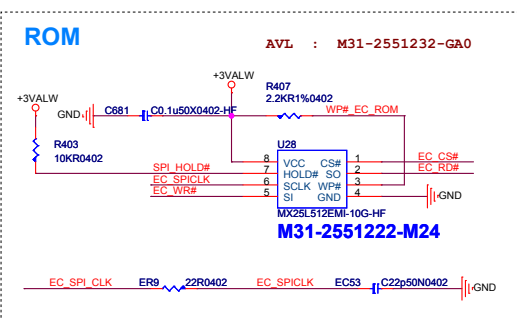
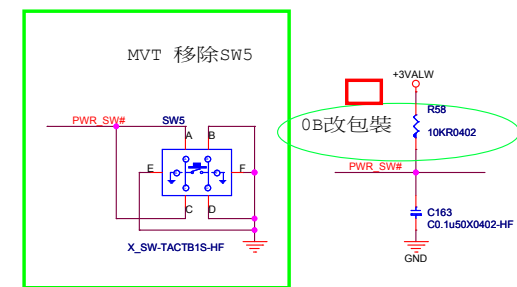
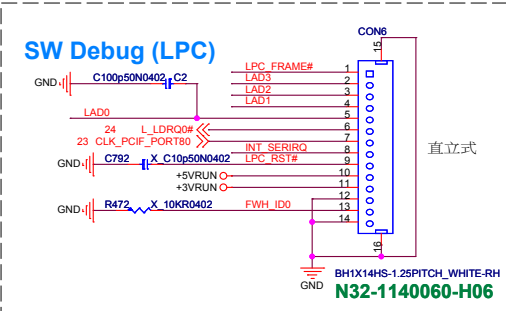
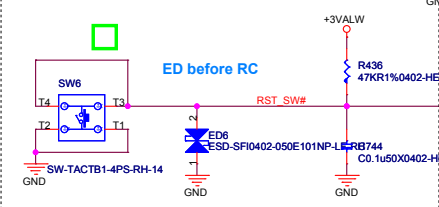
EPF021J Sink current not enough, only using BSS138 (0.22A)



LED Keyboard CONN



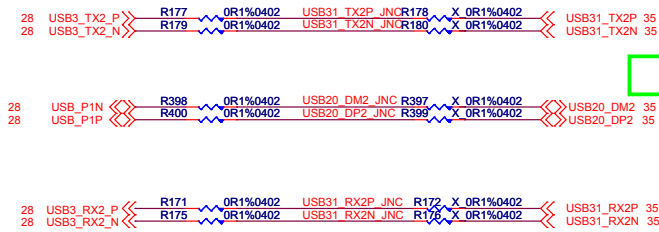
## Hardware Reset





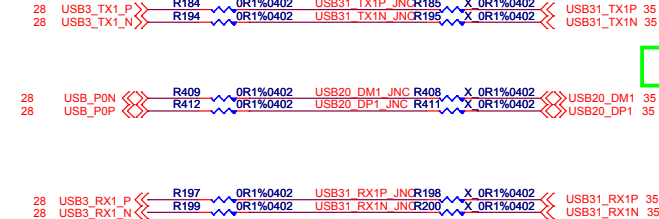
# USB 3.0 Port 1

PCH ASM1142

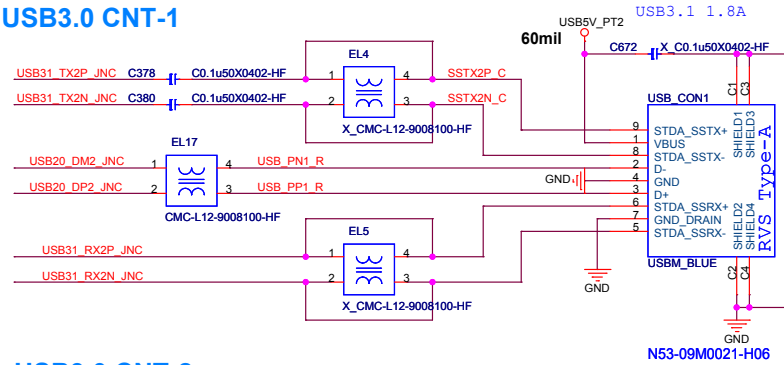


# USB 3.0 Port 2

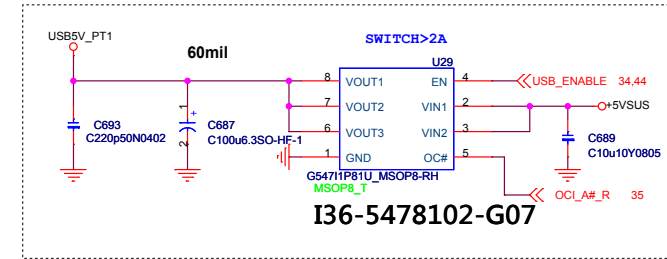
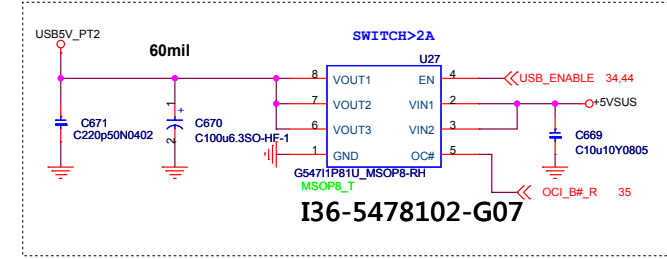
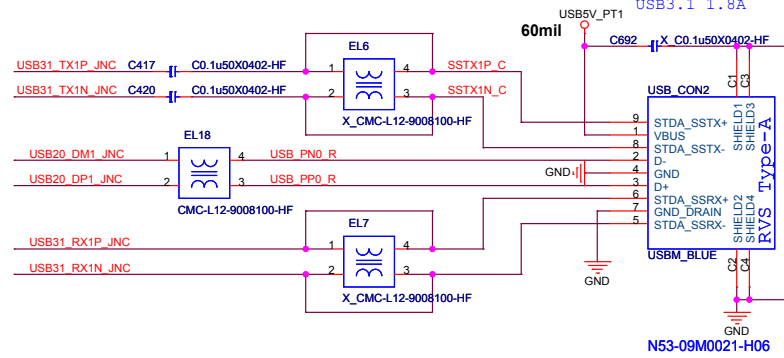
PCH ASM1142



## USB3.0 CNT-1

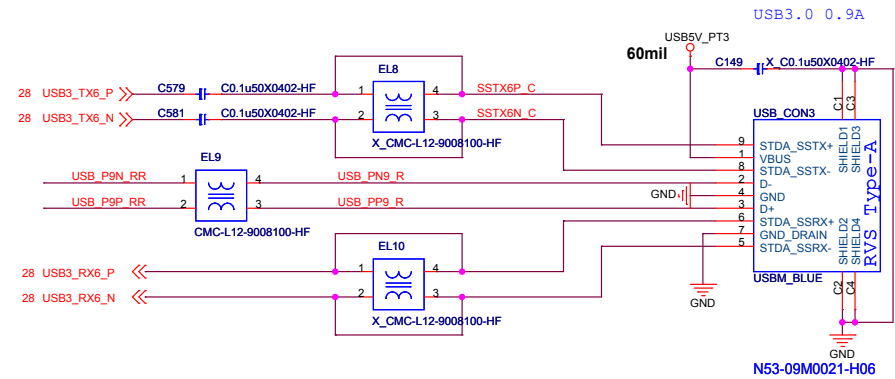
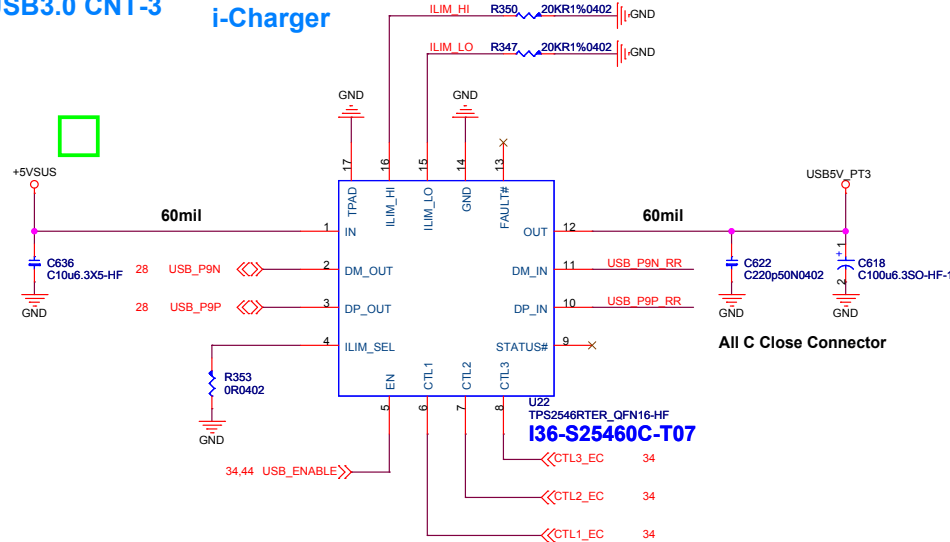


## USB3.0 CNT-2



## USB3.0 CNT-3

i-Charger

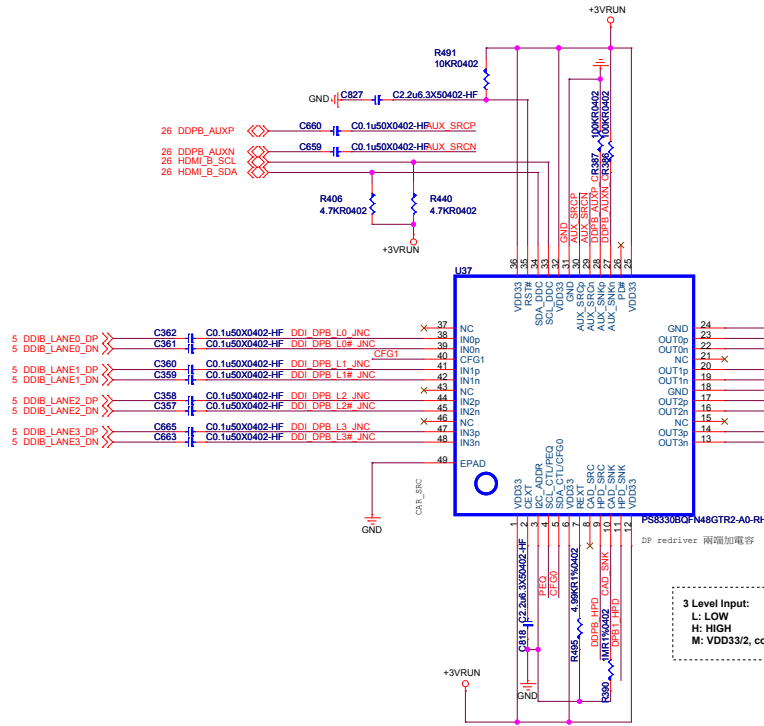
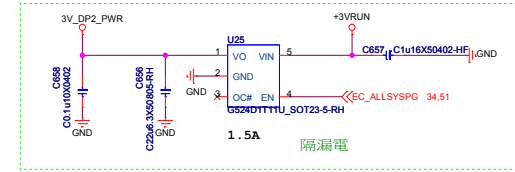
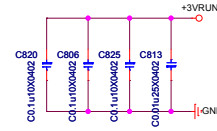


msi MICRO-STAR INT'L CO.,LTD.			
Title	USB 3.0 /iCharger		
Size	Document Number	Rev	
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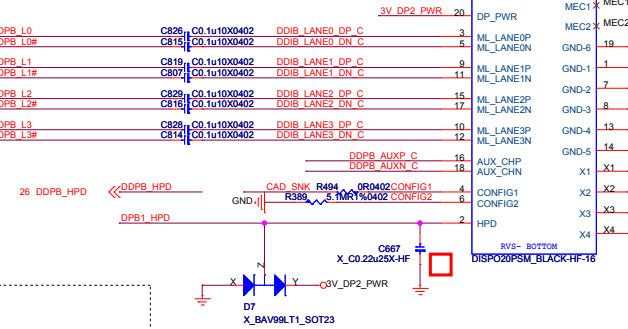
## Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP\_PWR pin and 1.5A at the Downstream device connector DP\_PWR pin.

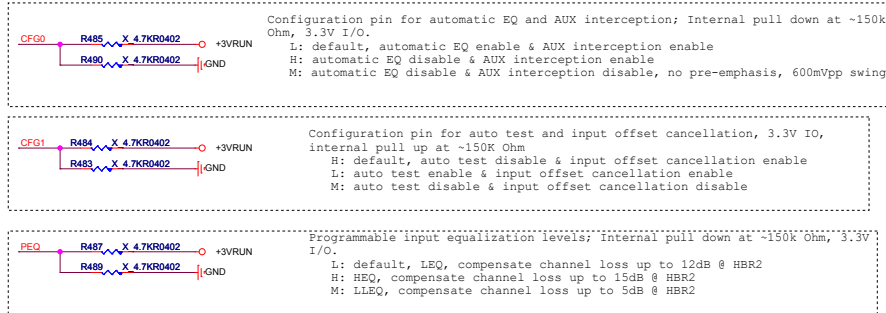


ESD Contact  $\pm 5$  KV & Air  $\pm 15$  KV

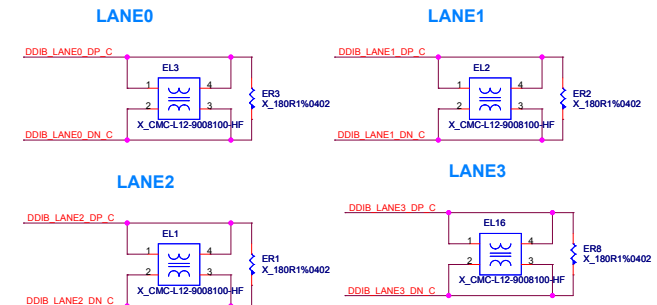
## Display Port



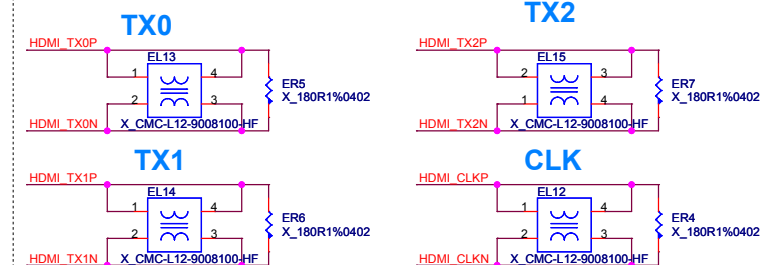
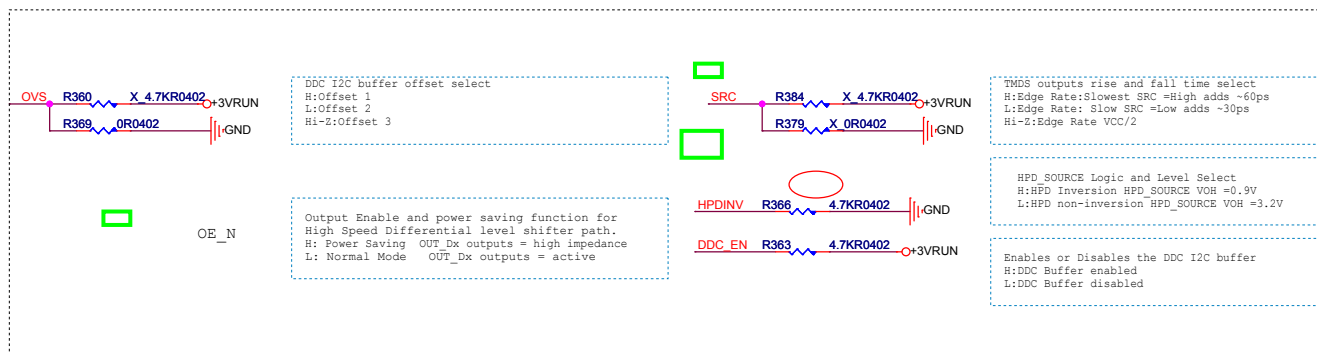
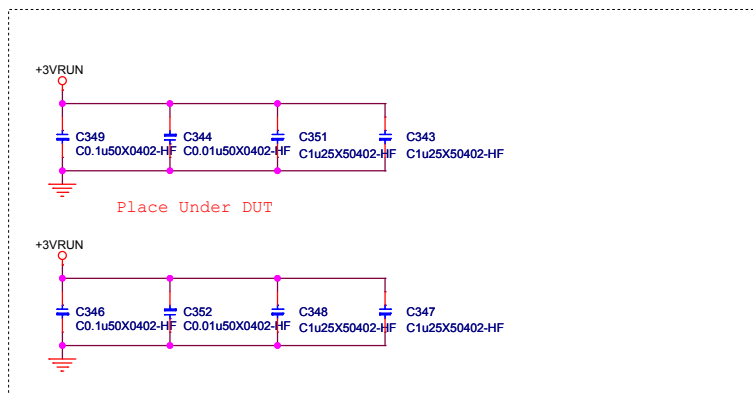
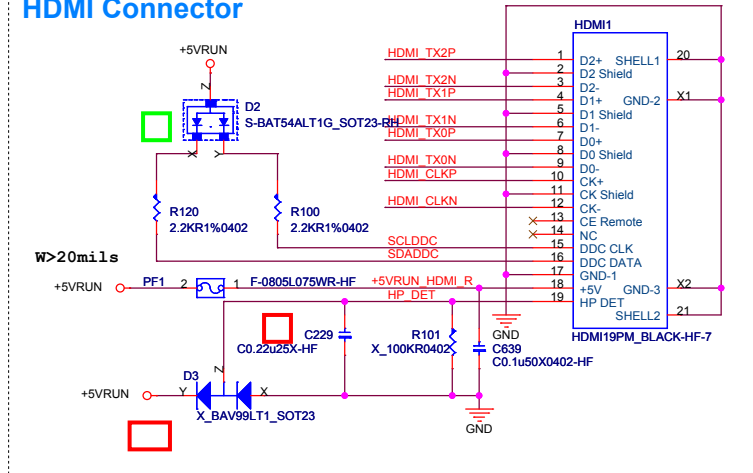
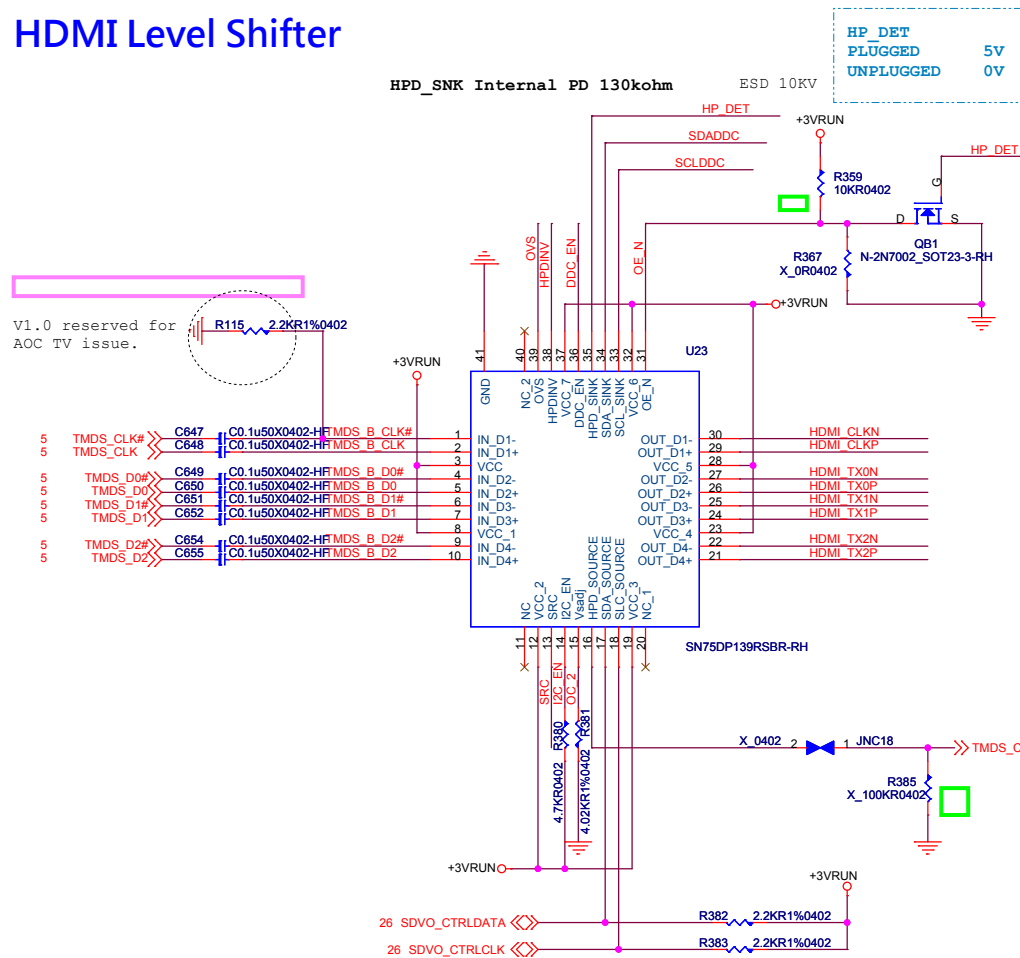
3 Level Input:  
L: LOW  
H: HIGH  
M: VDD3/2, connect both pull-up and pull-down resistors



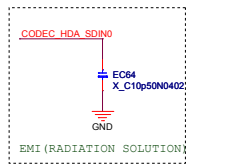
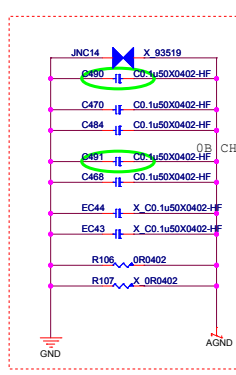
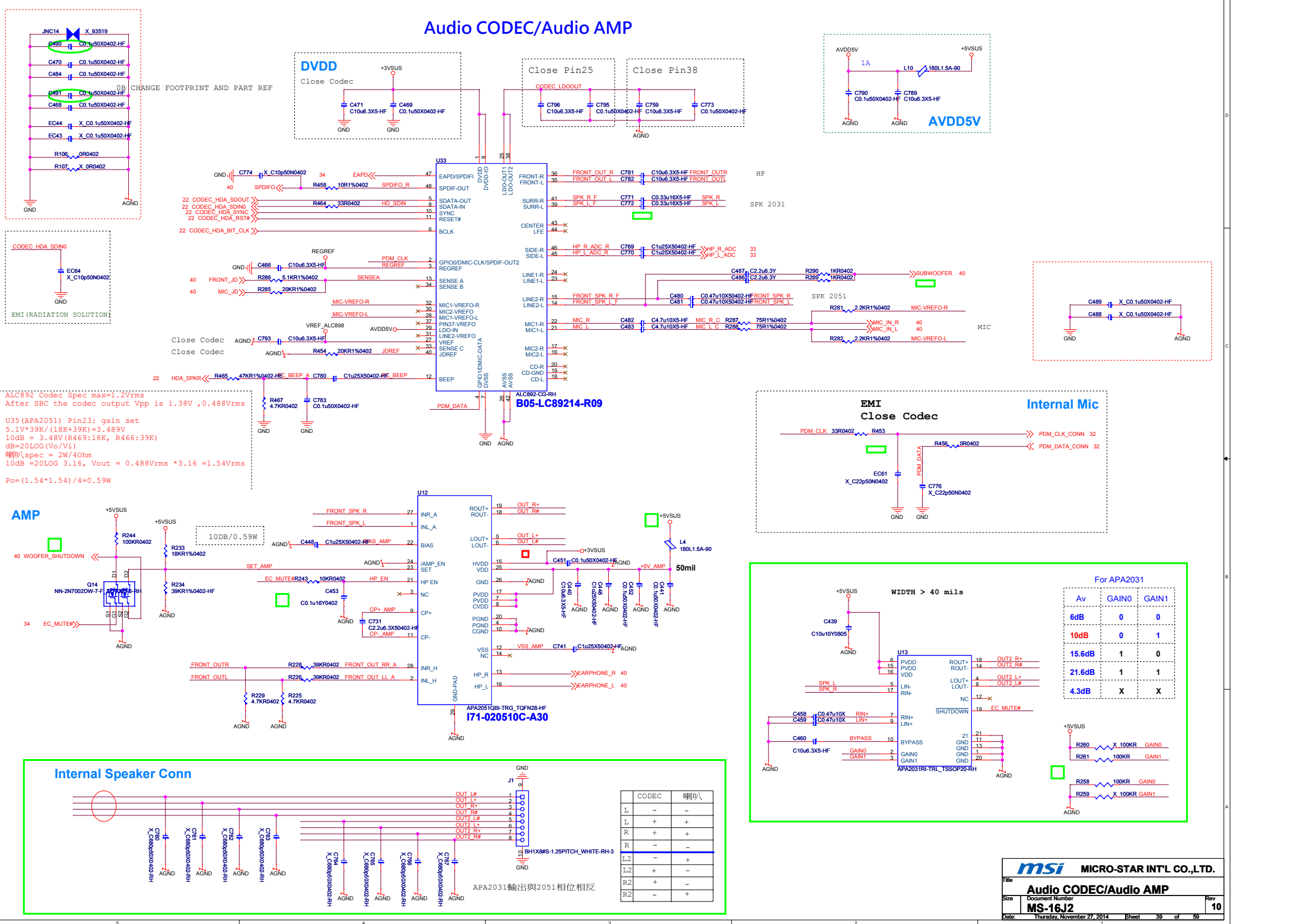
## EMI Close Connector



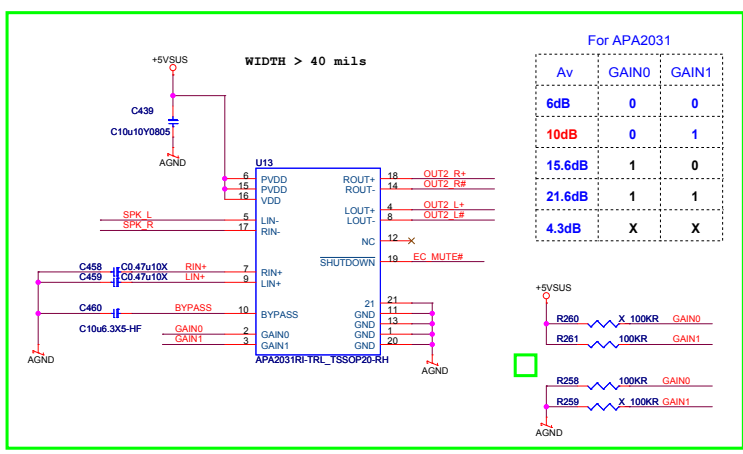
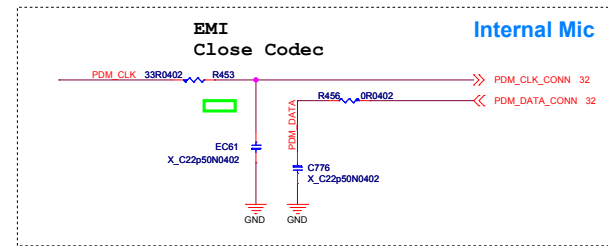
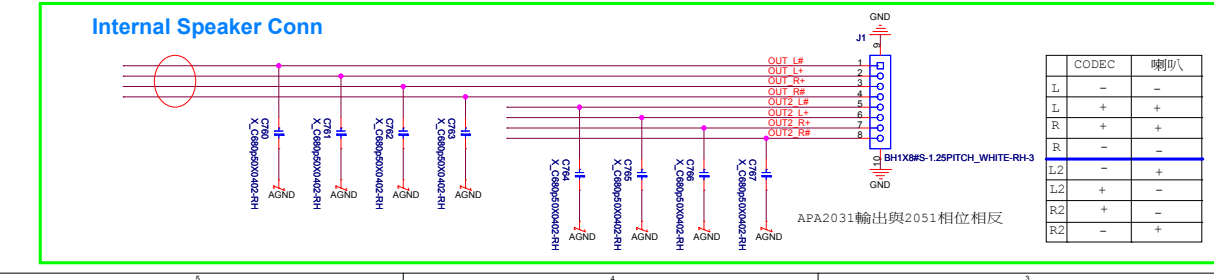
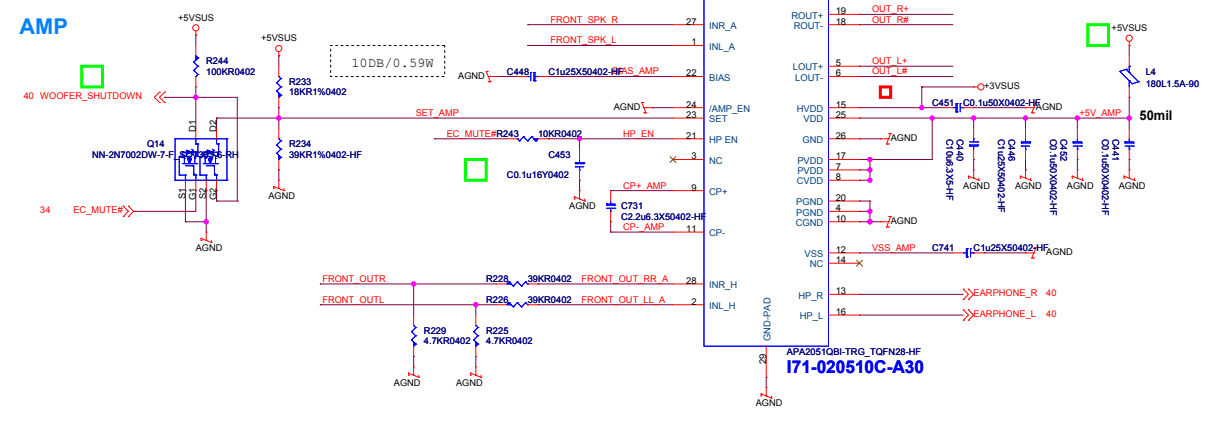
## HDMI Level Shifter



# Audio CODEC/Audio AMP

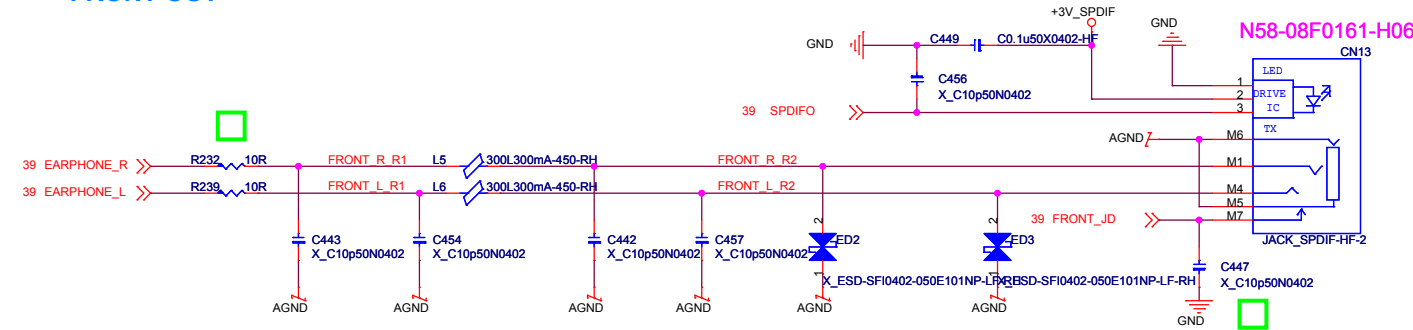


ALC892 Codec Spec max=1.2Vrms  
After SBC the codec output Vpp is 1.38V, 0.488Vrms  
U35 (APA2051) Pin23: gain set  
5.1V\*39K/(18K+39K)=3.489V  
10dB = 3.48V (R469:18K, R466:39K)  
dB=20LOG (Vo/Vi)  
喇叭\spec = 2W/4ohm  
10dB = 20LOG 3.16, Vout = 0.488Vrms \*3.16 =1.54Vrms  
Po=(1.54\*1.54)/4=0.59W

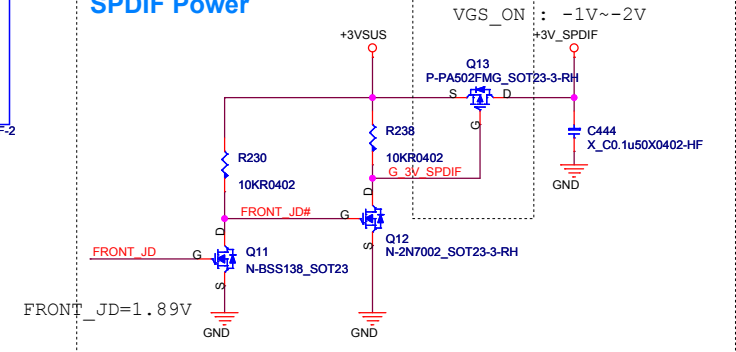


# Audio CONN /Woffter

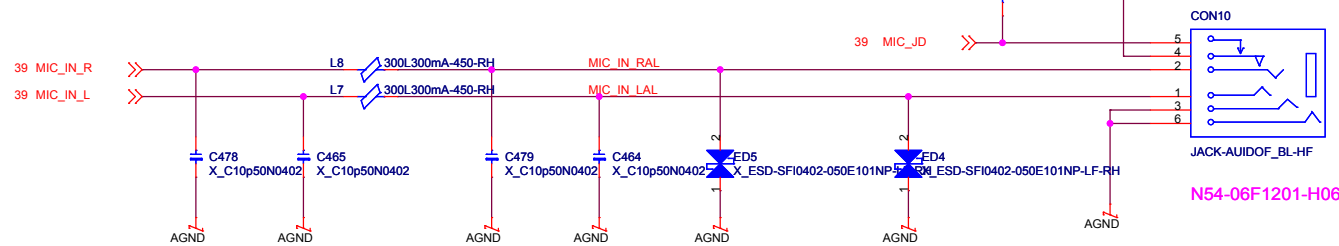
## FRONT OUT



## SPDIF Power



## MIC IN

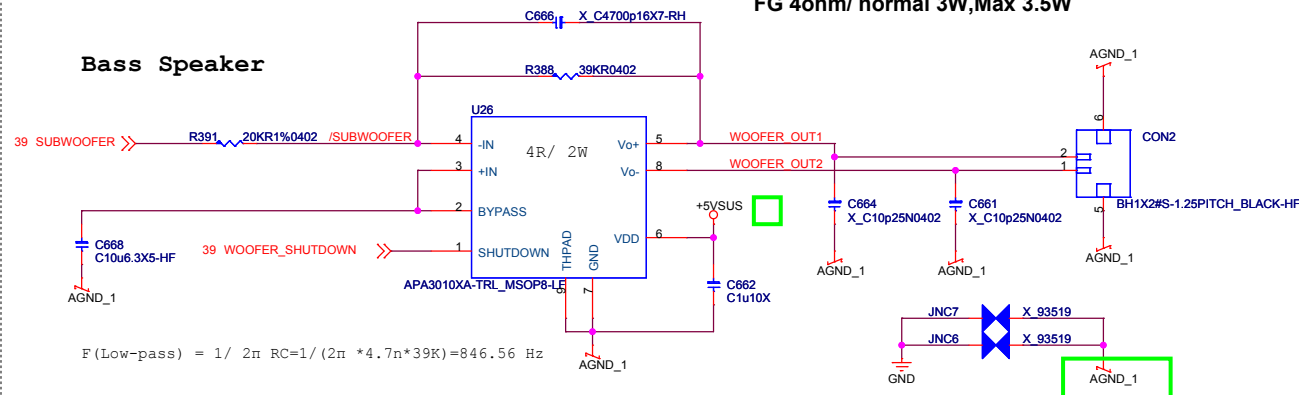


ALC892 SPC MAX 為 1.2Vrms  
gain= -2\*(R370/R371)= -2\*(40K/20K) = -4

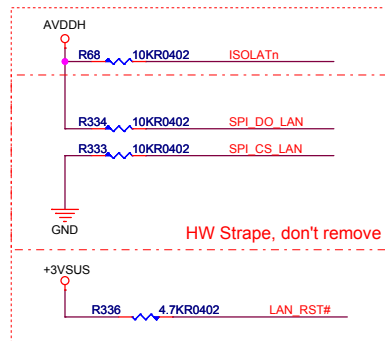
Vout= 0.58Vrms \* 4 = 2.32Vrms , Po=(2.32\*2.32)/3.8=1.42W

**Woofer SPEC**  
YG 3.8ohm / normal 3W,Max 3.5W  
FG 4ohm/ normal 3W,Max 3.5W

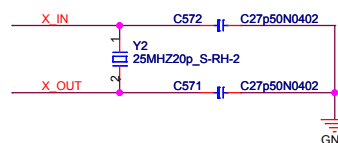
## Bass Speaker



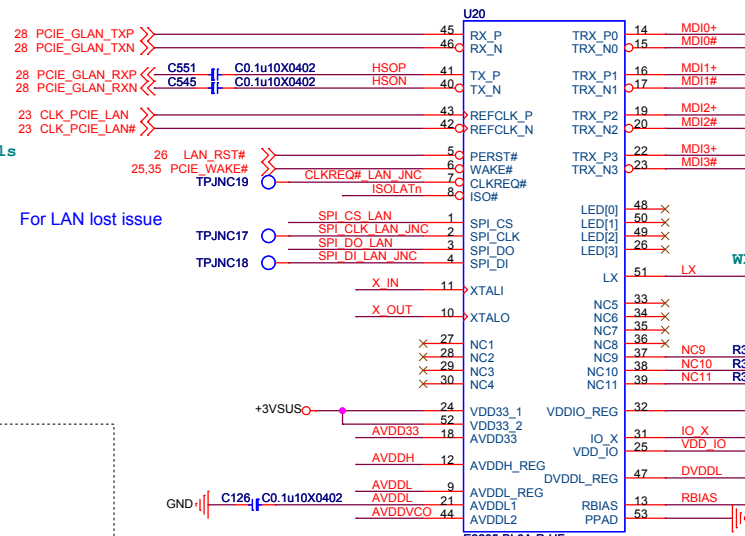
## GIGA LAN(BigFoot BFN2205B)



RST# spacing 20mils

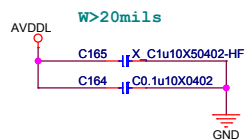


For LAN lost issue

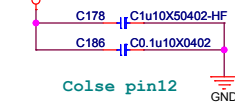


**B06-E22050C-Q24**

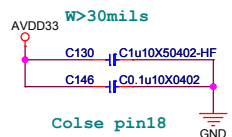
MAC 燒 CHIP 內  
，有次數限制



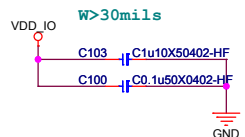
AVDDH W>20mils



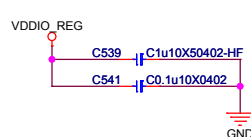
Colse pin:



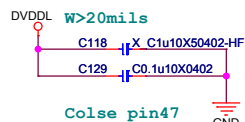
Colse pin18



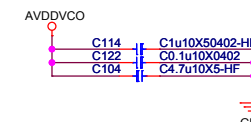
W>30mils



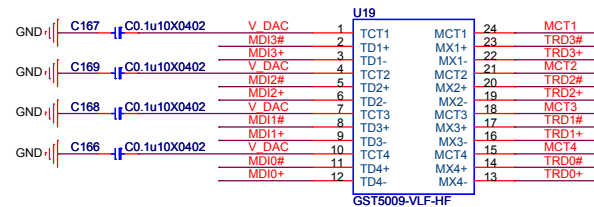
VBBIO 050



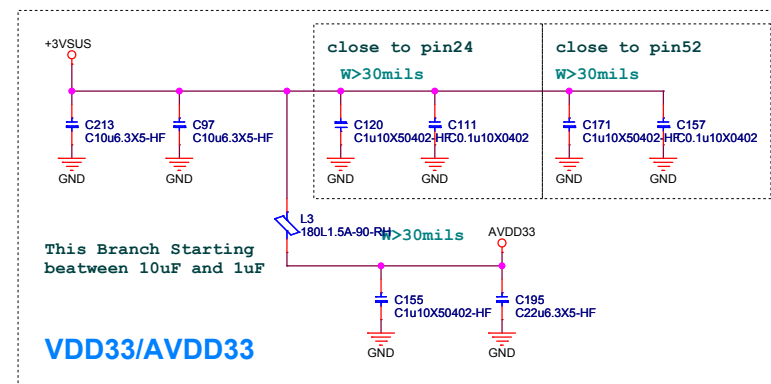
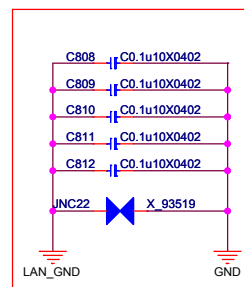
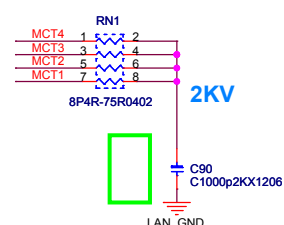
Colse pin4



AVDDVCO

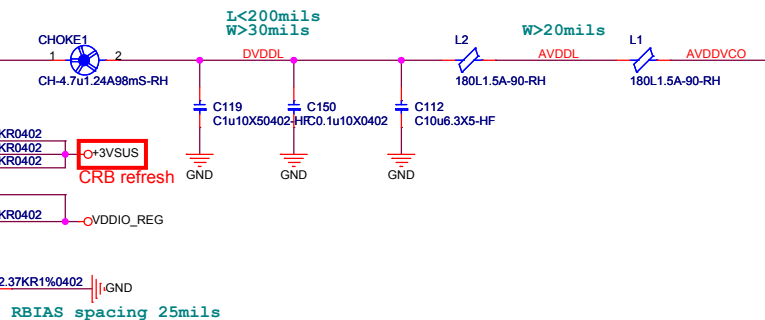


**L05-0200150-B09**

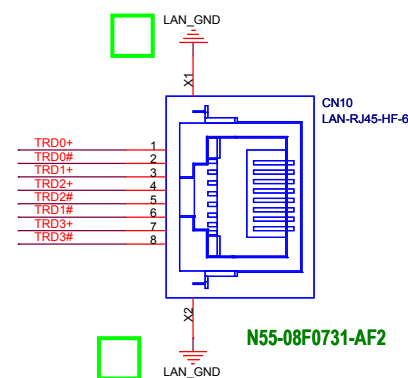


This Branch Starting  
between 10uF and 1uF

## VDD33/AVDD33

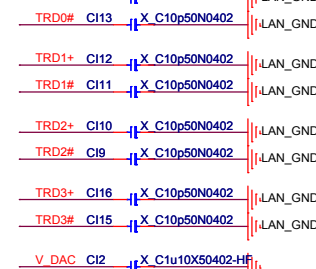


RBIAS spacing 25mils

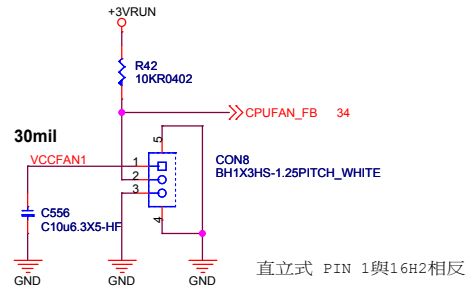
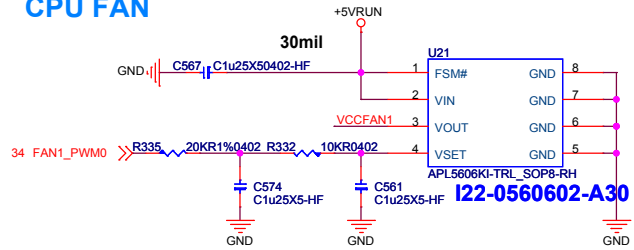


**N55-08F0731-AF2**

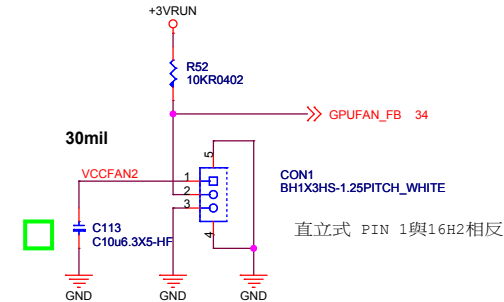
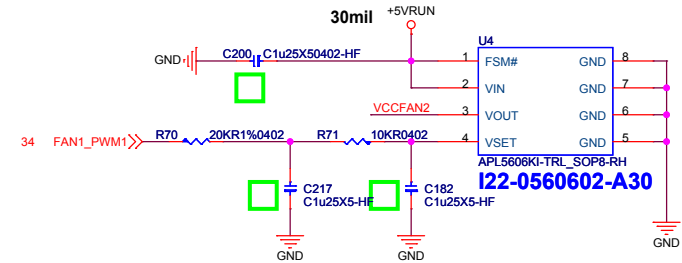
EMI



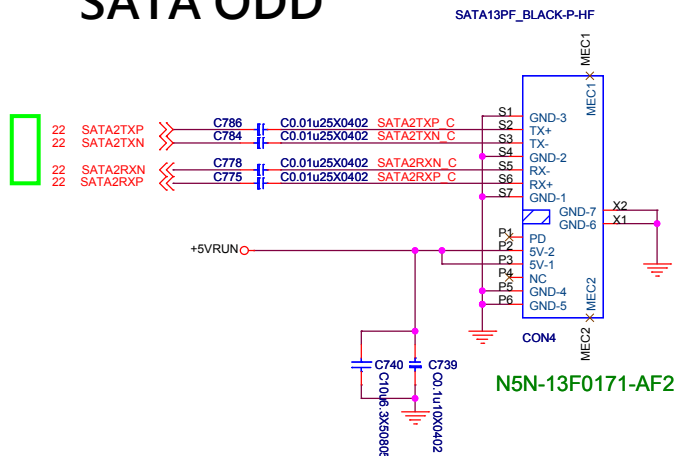
## CPU FAN



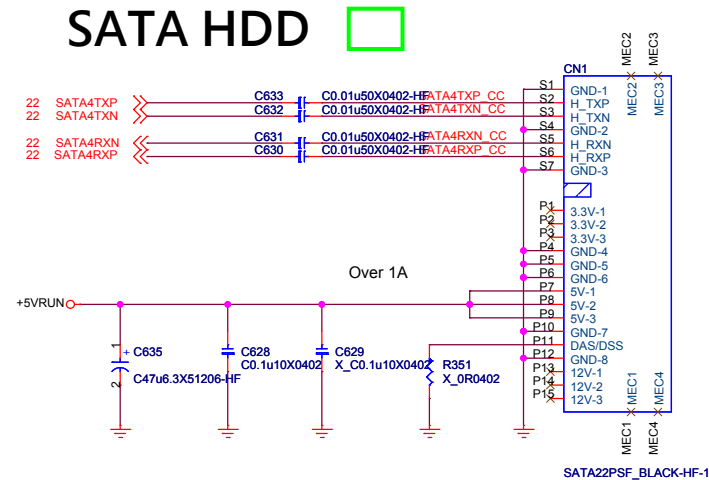
## DGPU FAN



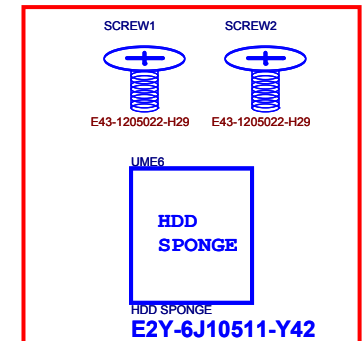
## SATA ODD



## SATA HDD

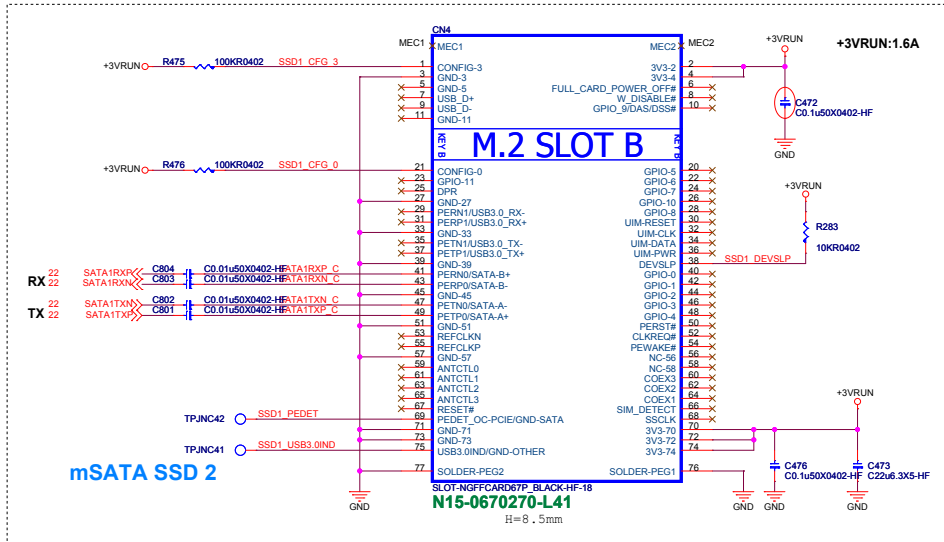


- 22. GND
- 21. TX
- 20. TX#
- 19. GND
- 18. RX#
- 17. RX
- 16. GND
- 15. V33
- 14. V33
- 13. V33
- 12. GND
- 11. GND
- 10. GND
- 9. V5
- 8. V5
- 7. V5
- 6. GND
- 5. Reserved
- 4. GND
- 3. V12
- 2. V12
- 1. V12

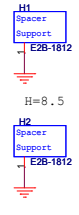


## SSD

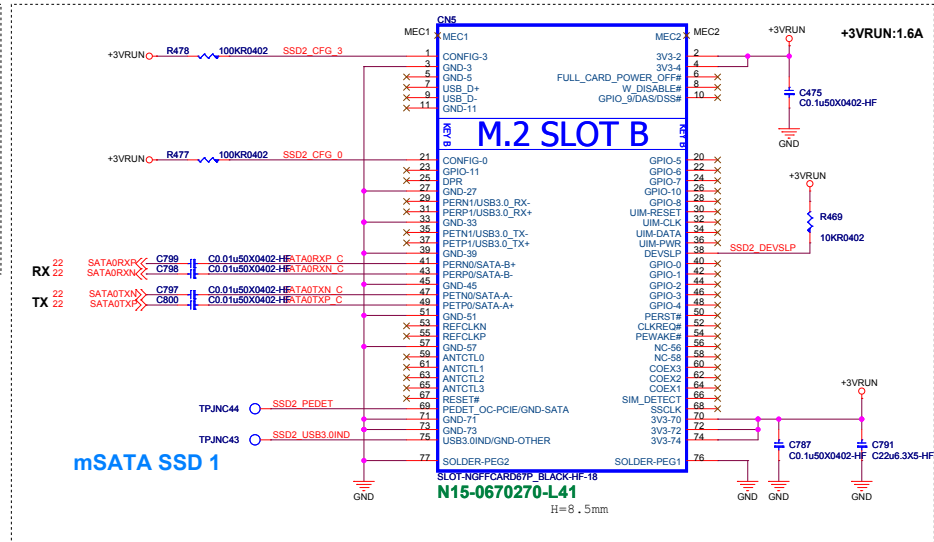
## SATA SIGNAL



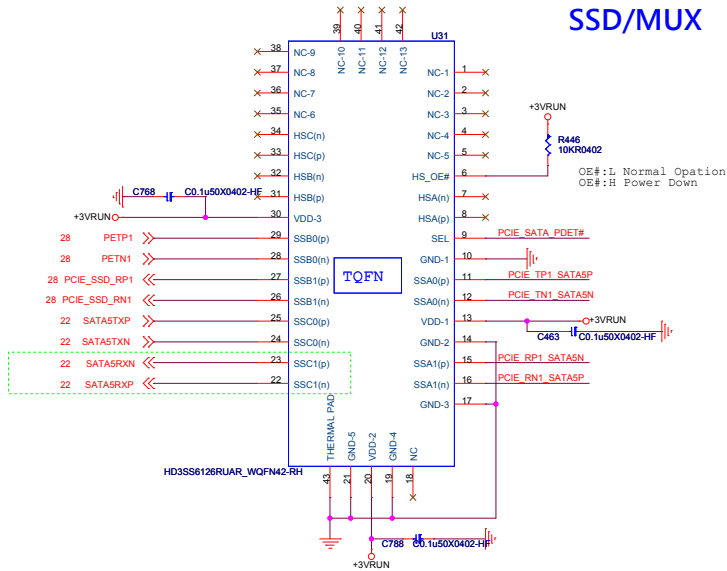
STAND OFF



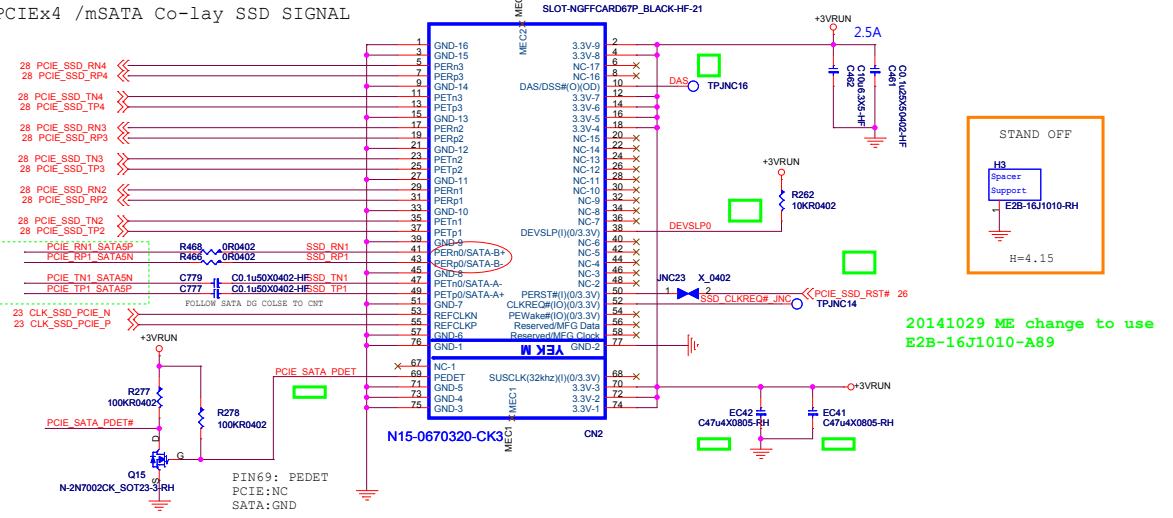
## SATA SIGNAL



## SSD/MUX



## PCIEx4 /mSATA Co-lay SSD SIGNAL



## PCIEx4 /SATA SSD3

中間 H=3.2mm

## TRUTH TABLE USB 3.0 SuperSpeed USB

SEL	USB 3.0 Port Selection		
	SSA0/1	SSB0/1	SSC0/1
0	To/From SSB0/1	To/From SSA0/1	Off
1	To/From SSC0/1	Off	To/From SSA0/1

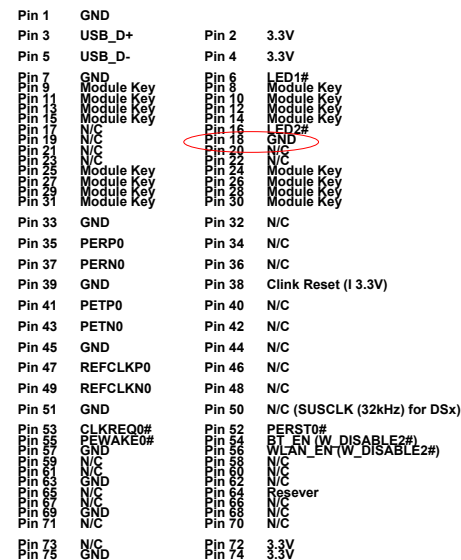
MSI MICRO-STAR INT'L CO.,LTD.

File: **SSD/MUX**

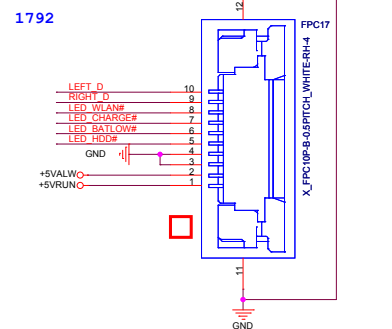
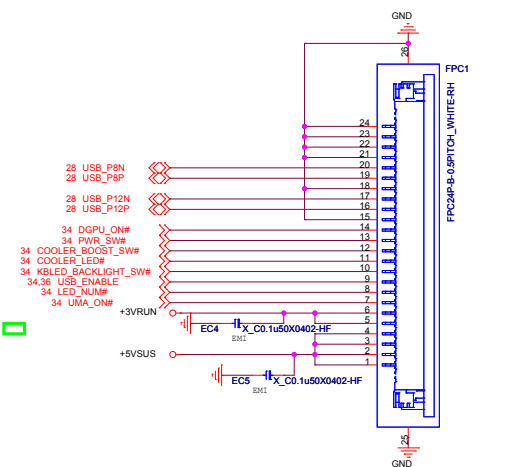
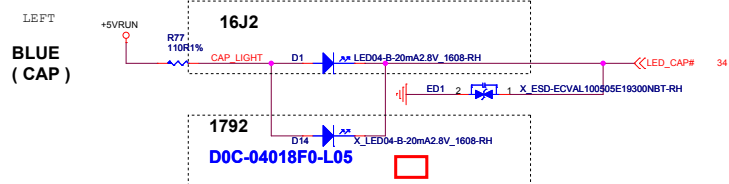
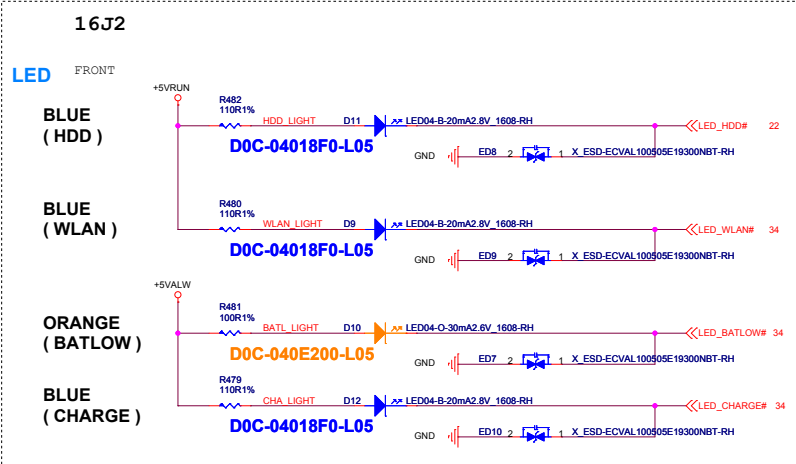
Size: Document Number **MS-16J2**

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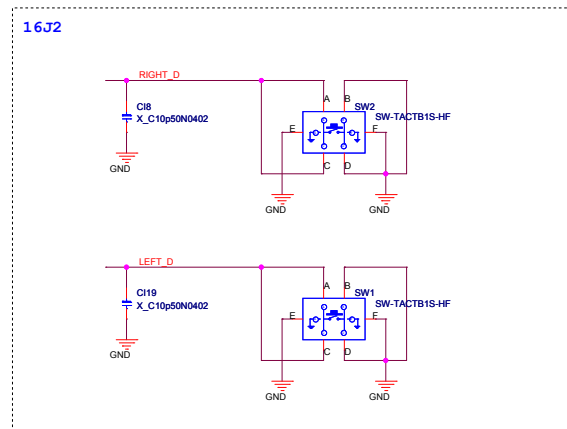
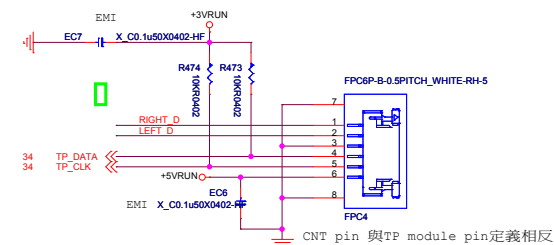




1792不上件



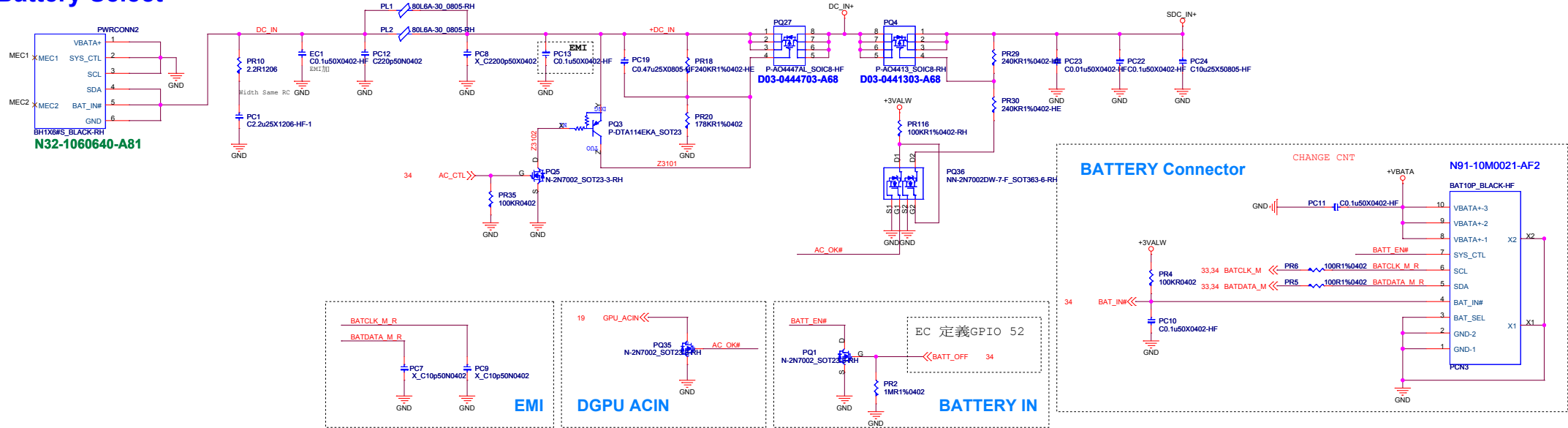
## Touch Pad



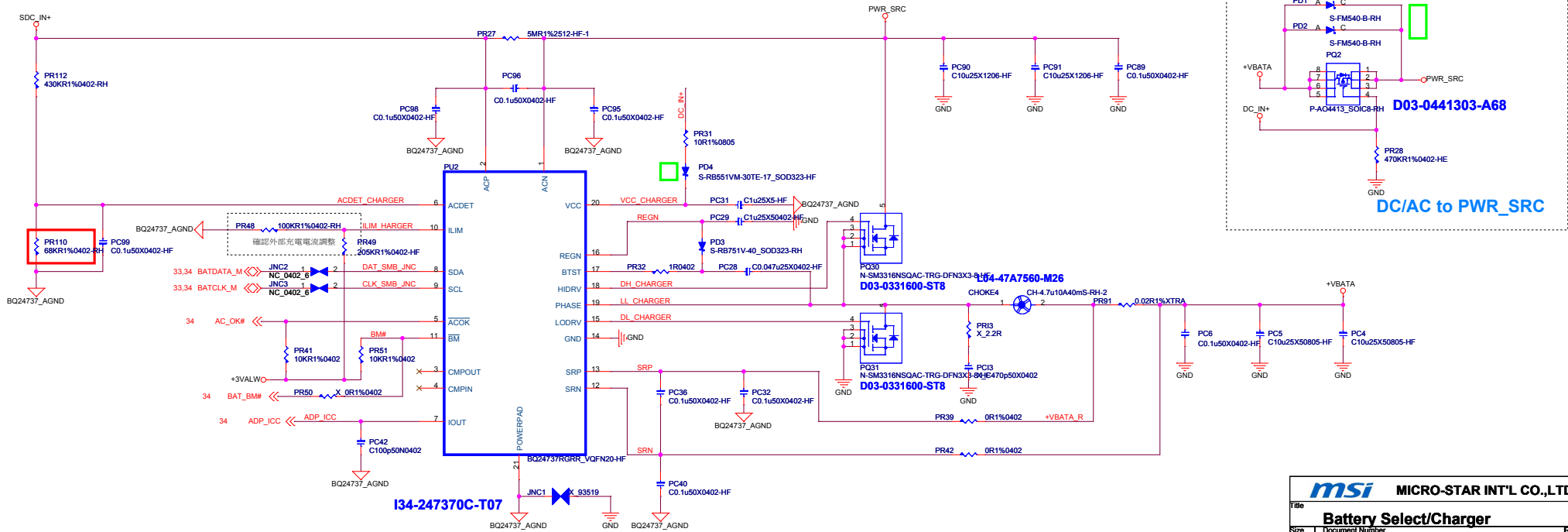


## Battery Select/Charger

## Battery Select



## Battery Charger



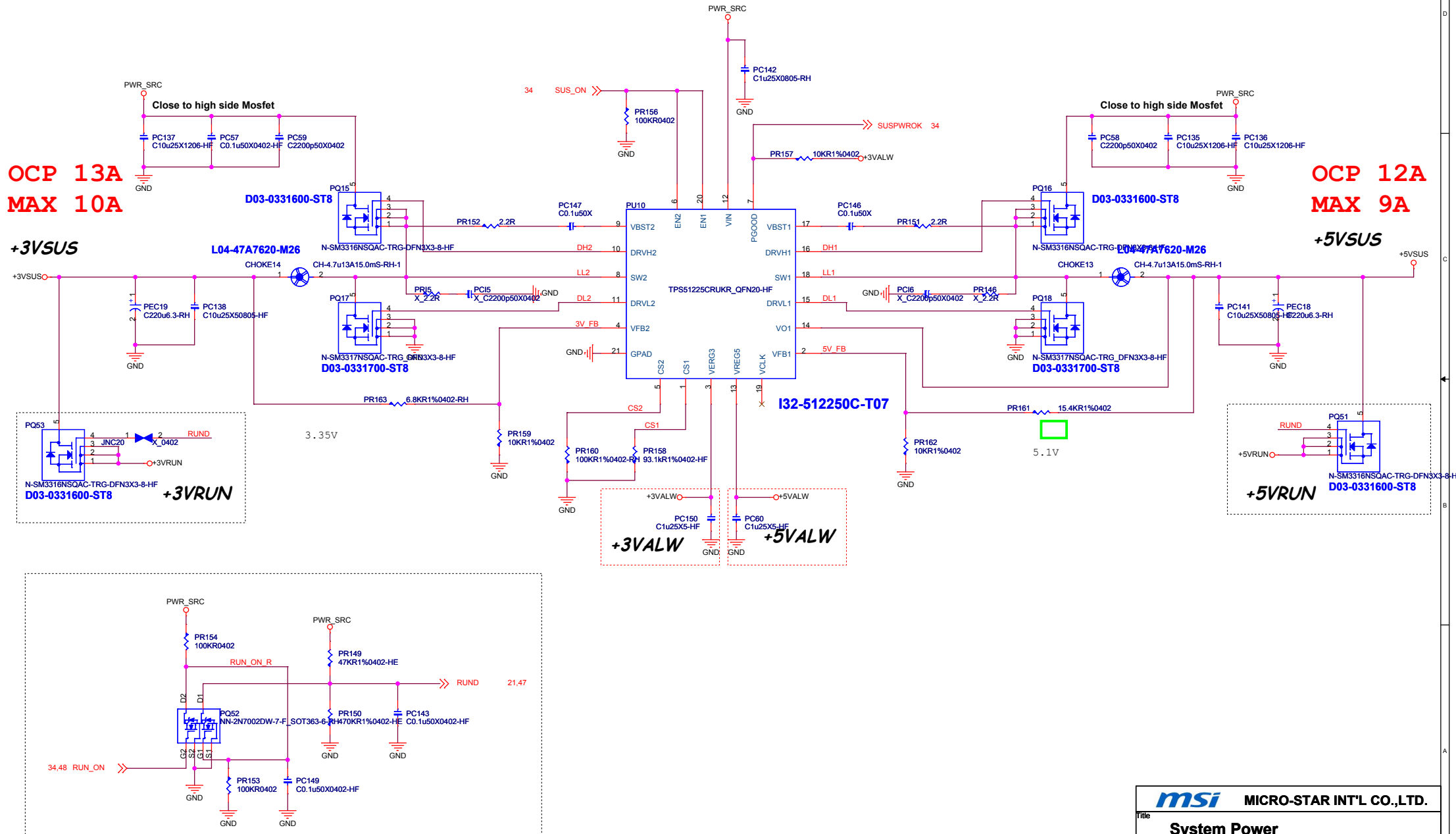
# System Power

**OCF 13A  
MAX 10A**

**+3VSUS**

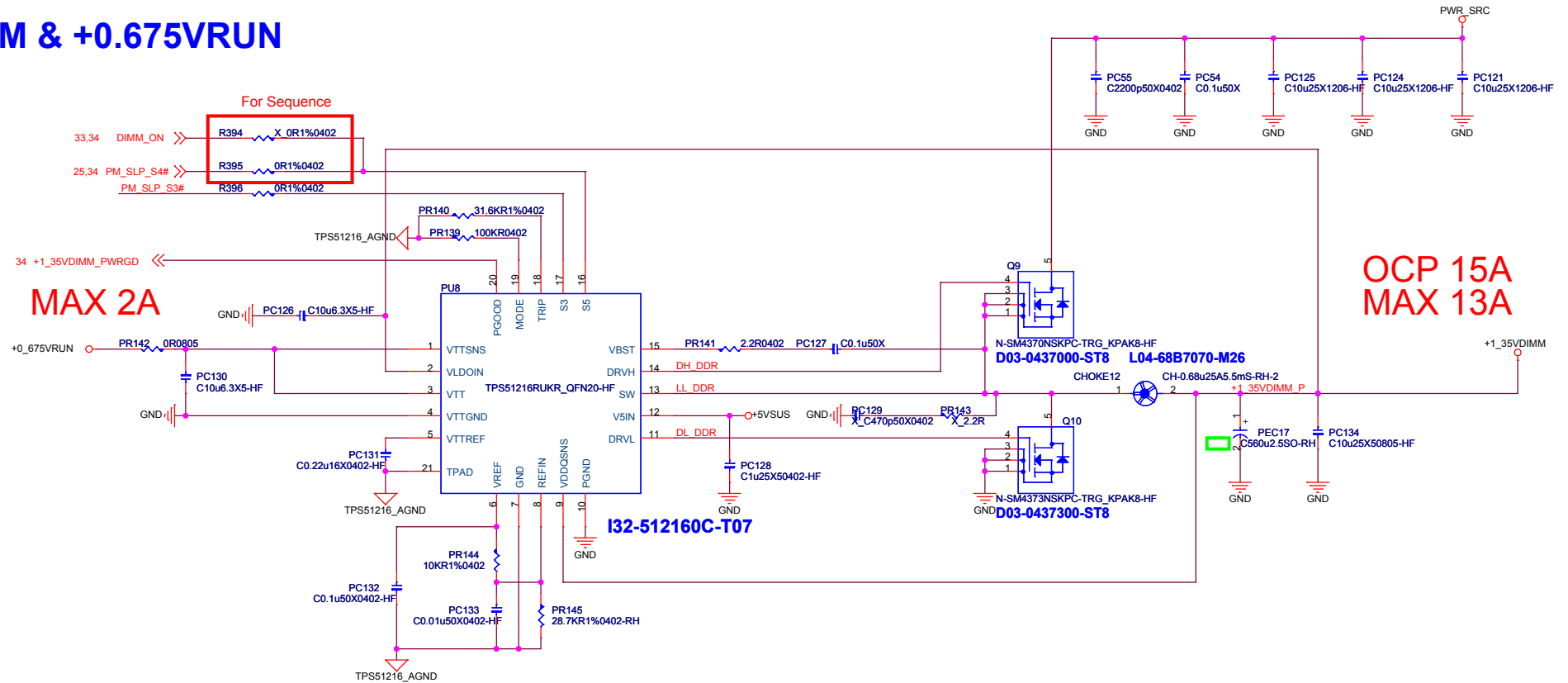
**OCF 12A  
MAX 9A**

**+5VSUS**

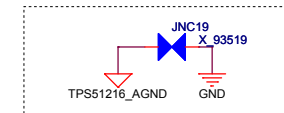
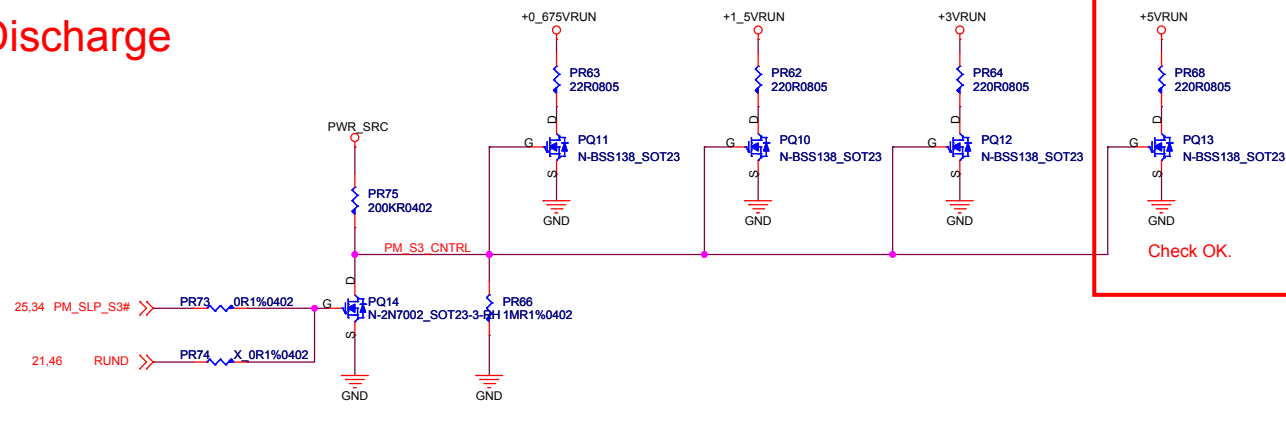


# +1.35VDIMM/+0.675VRUN

## +1.35VDIMM & +0.675VRUN

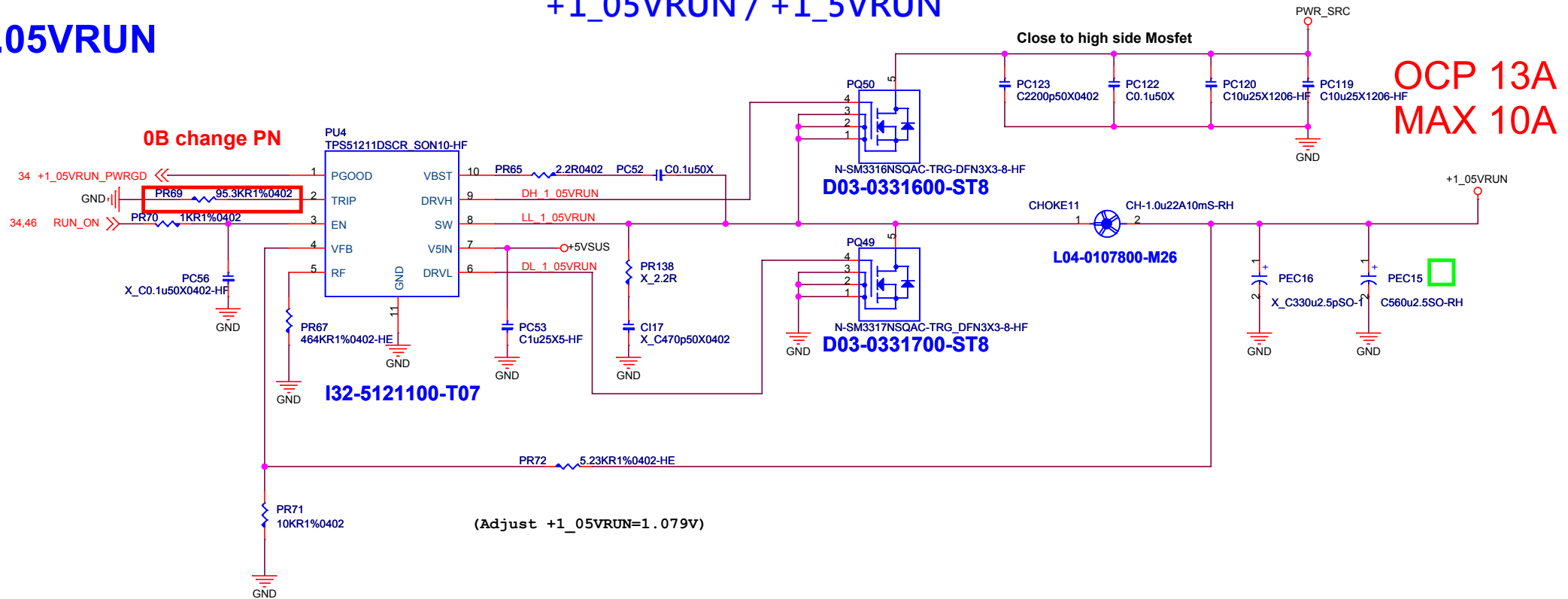


## Discharge



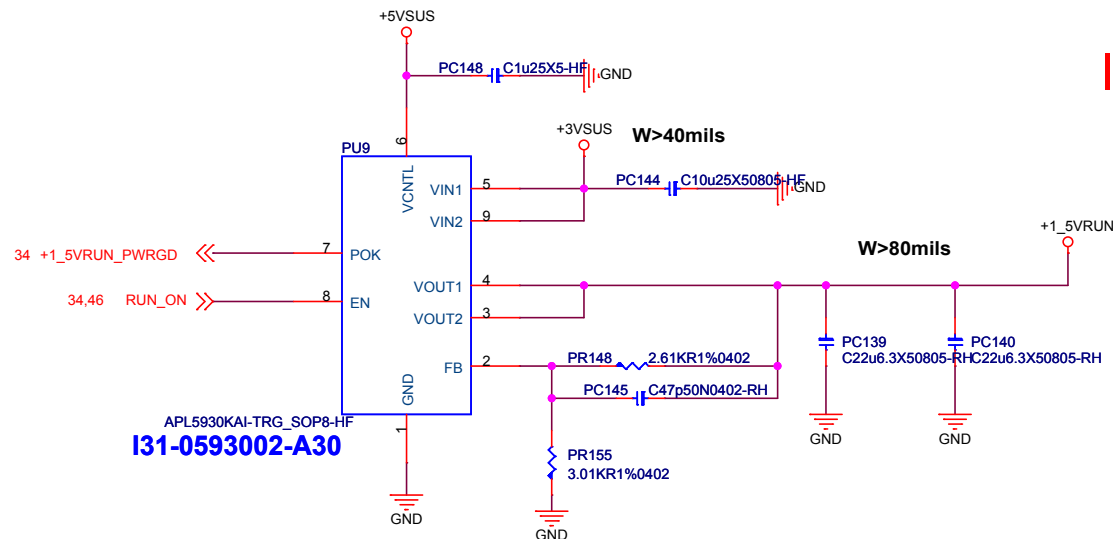
# +1.05VRUN

## +1\_05VRUN / +1\_5VRUN



OCP 13A  
MAX 10A

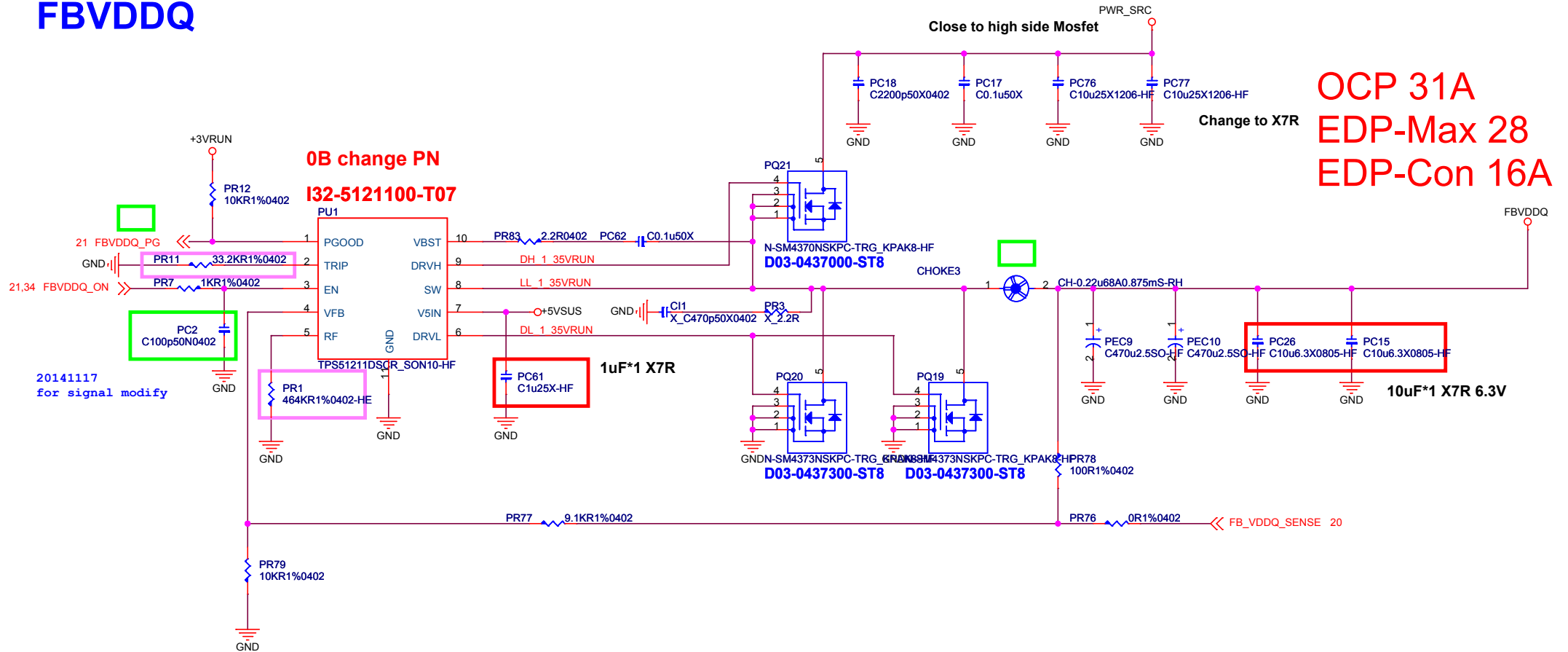
# +1.5VRUN



IC MAX 3A  
253mA

msi MICRO-STAR INT'L CO.,LTD.			
Title			
+1_05VRUN / +1_5VRUN			
Size	Document Number		Rev
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Date:	Thursday, November 27, 2014		Sheet 48 of 59

# FBVDDQ



# DGPU POWER / UP1642PQAG

EDP-Peak 85A

EDP-MAX 50A

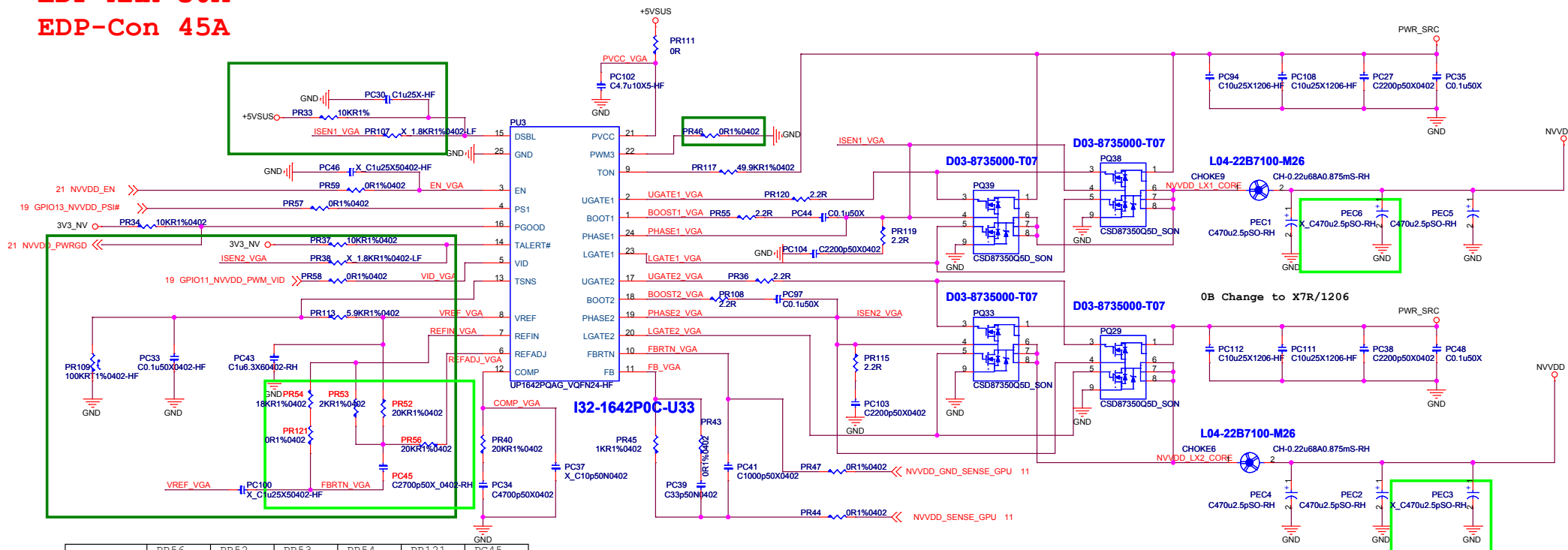
EDP-Con 45A

# DGPU POWER NVVDD

CONFIG A

VBoot:0.875V

Vmin:0.6V / Vmax:1.2V



	PR56	PR52	PR53	PR54	PR121	PC45
CONFIG	R1	R2	R3	R4	R5	C
N16E-GT						
N16P-GX-B	20K	20K	2K	18K	0	2.7nF

20141029 power modify for GPU power setting

PR52,PR56: 39K ohm to 20K ohm

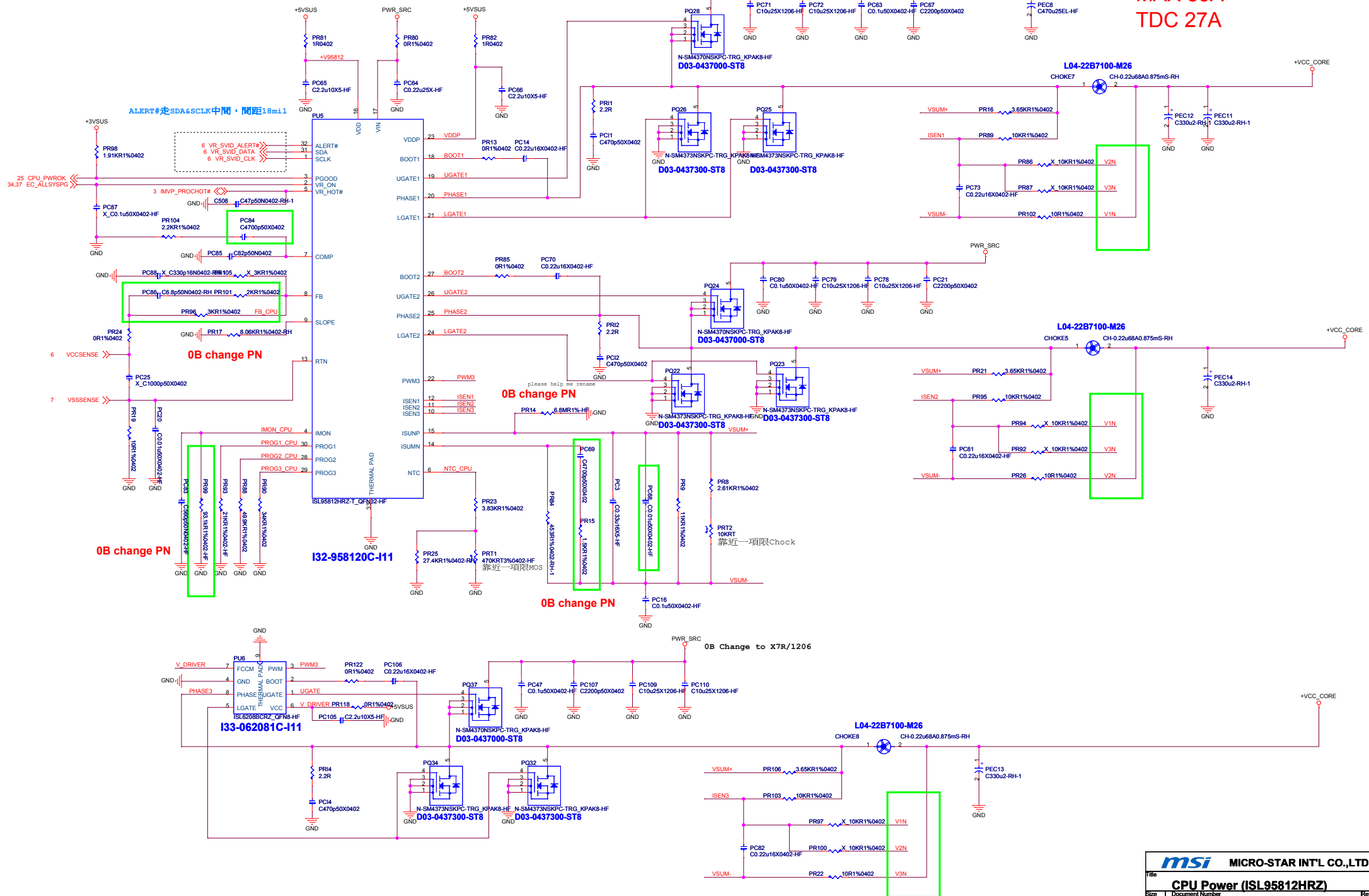
PR53: 1.5K ohm to 2K ohm

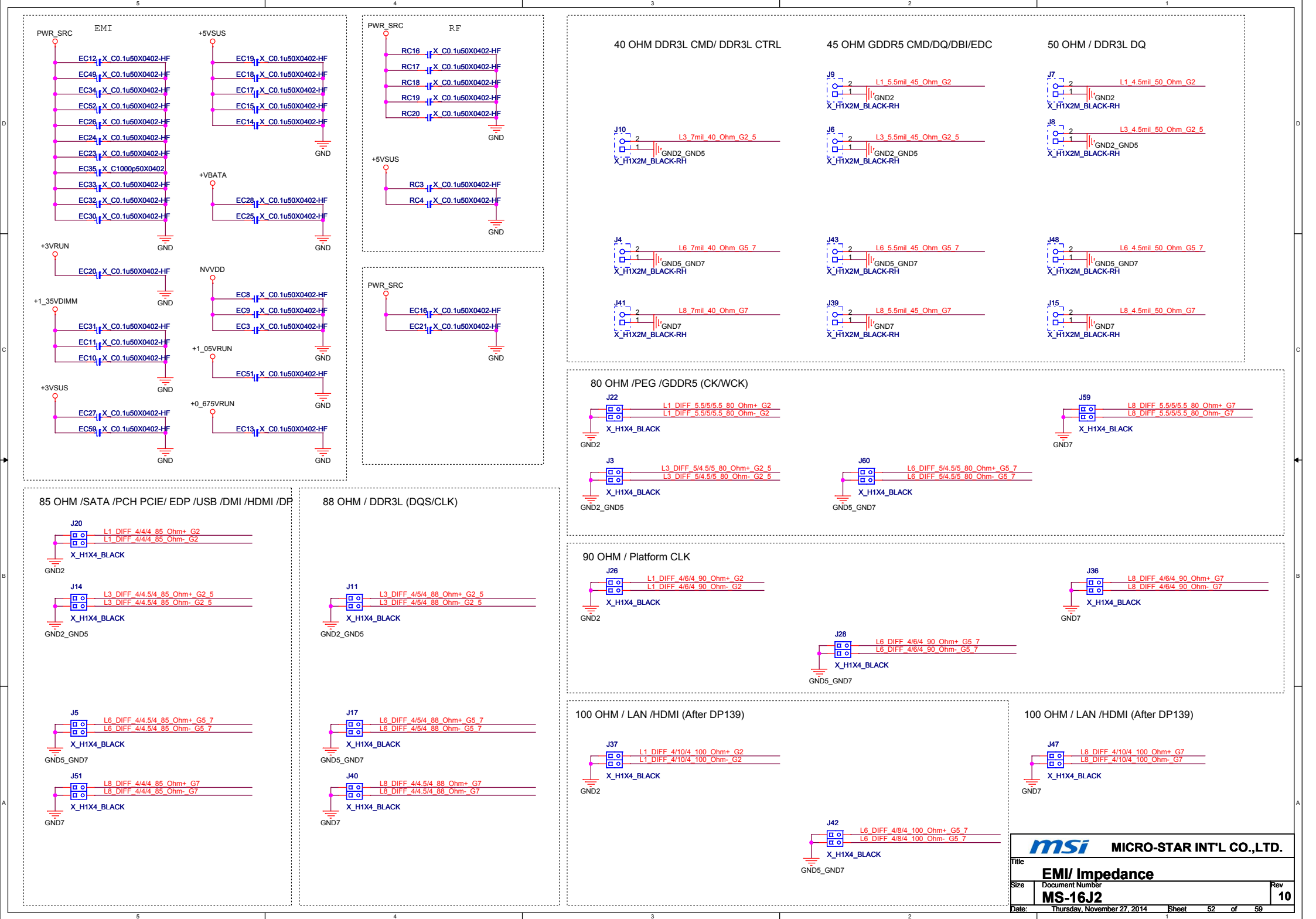
PR54: 30K ohm to 18K ohm

PR121: 1.5K ohm to 0 ohm

PC45: 1.5nF to 2.7nF

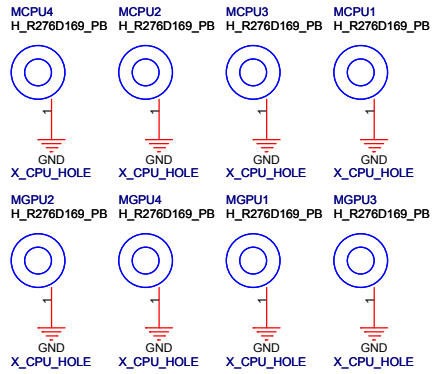
MAX 85A  
TDC 27A



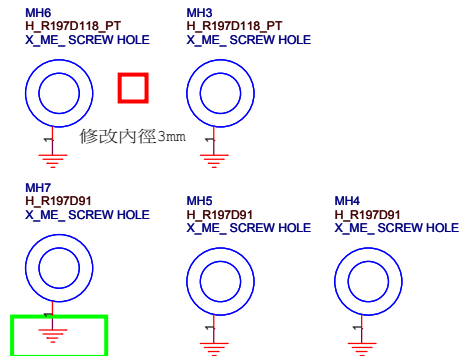




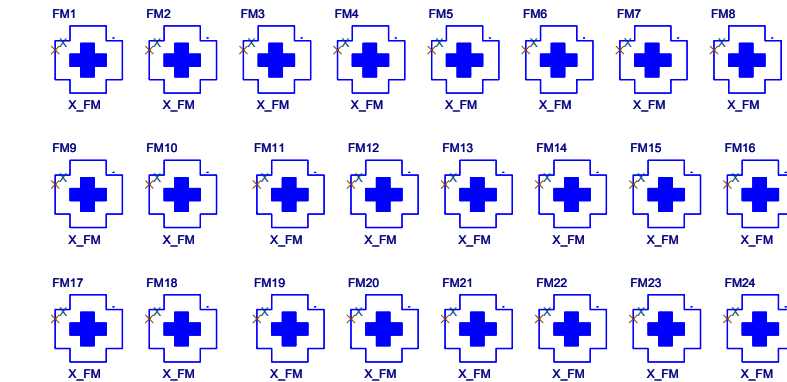
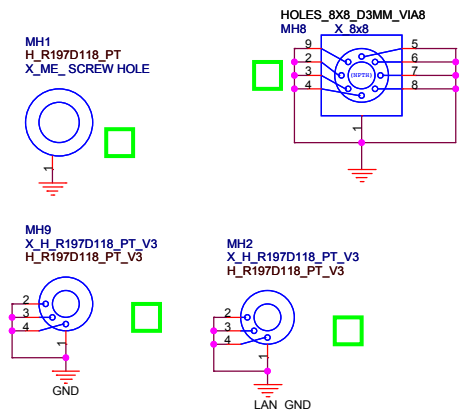
## CPU/GPU Holes



## OD 2.3

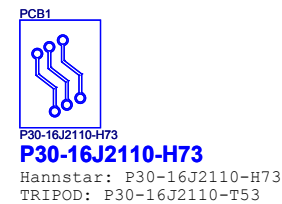
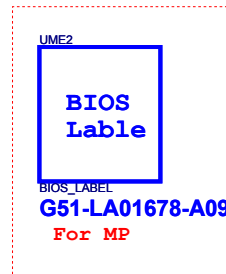
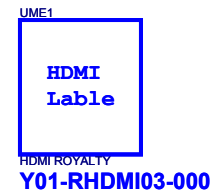
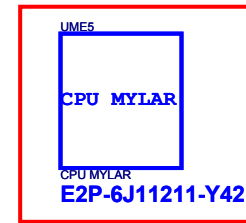
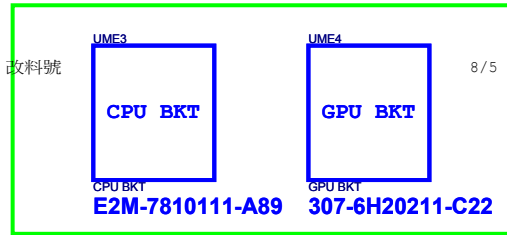


版邊 內3 / 外8



7/31 改料號

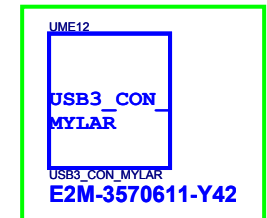
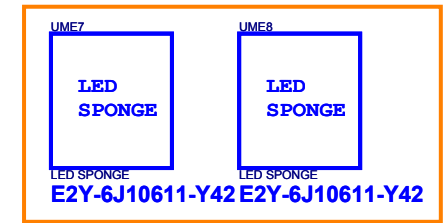
8/5 改料號



Only 1792

20141024 ME change to use E2M-3570611-Y42

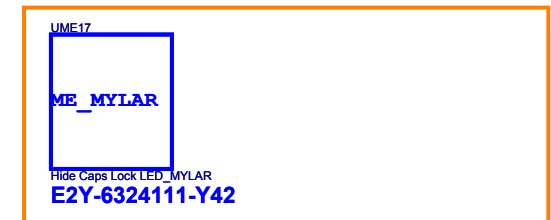
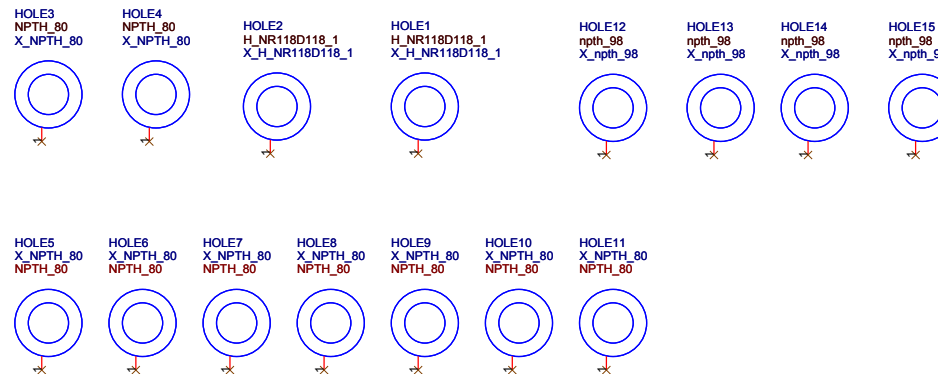
Only 16J2



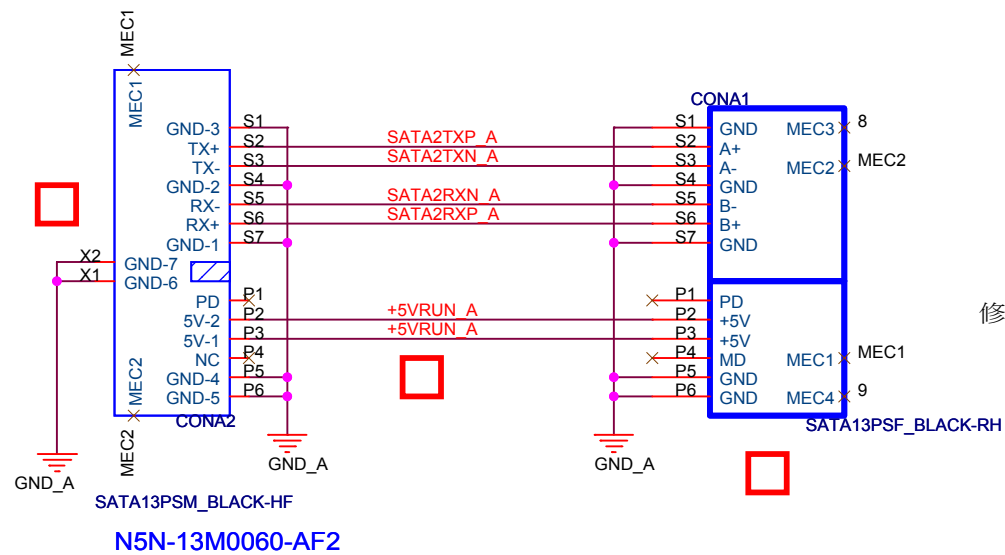
20141016 ME add  
20141024 ME change to use E2P-6J11411-Y42  
Only 16J2

20141020 EMI add

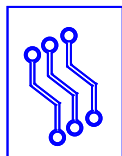
20141016 ME add UME9 and UME10  
20141120 ME delete UME9 and UME10



20141024 ME add E2P-6J11611-Y42  
20141028 ME add E2Y-6J10711-Y42  
20141120 ME add E2Y-6324111-Y42  
Only 16J2



### PCBA1

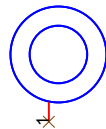


P30-16J2A10-H73

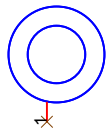
**P30-16J2A10-H73**

Hannstar: P30-16J2A10-H73  
TRIPOD: P30-16J2A10-T53

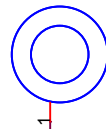
HB2  
X\_NPTH\_80  
NPTH\_80



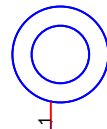
HB1  
X\_NPTH\_80  
NPTH\_80



MB1  
X\_H\_R197D91  
H\_R197D91



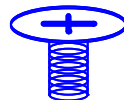
MB2  
X\_H\_R197D91  
H\_R197D91



GND\_A

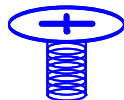
GND\_A

SCREWA2



**E43-1205003-H29**

SCREWA1



**E43-1205003-H29**

**msi**

**MICRO-STAR INT'L CO.,LTD.**

Title

**[A] 1792 ODD**

Size  
A4

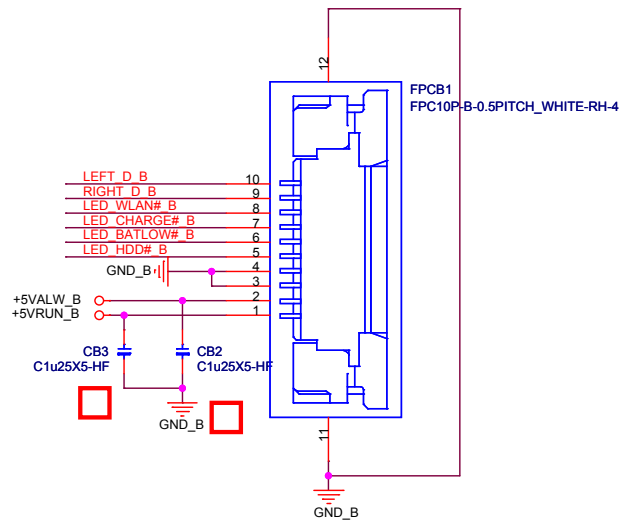
Document Number

**MS-16J2A**

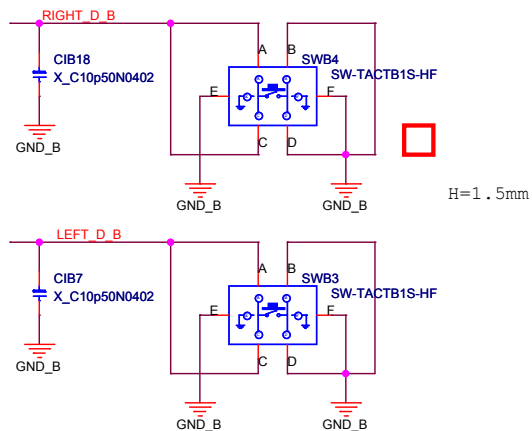
Rev  
10

Date: Thursday, November 27, 2014

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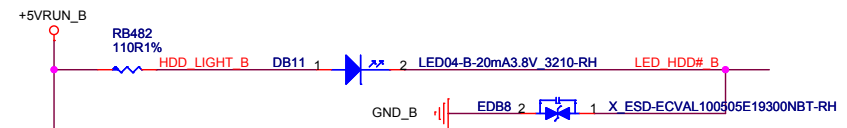
1792



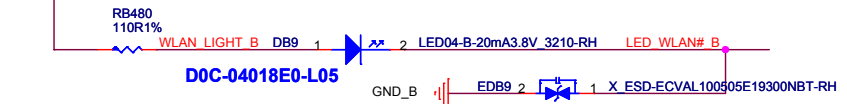
1792

LED FRONT

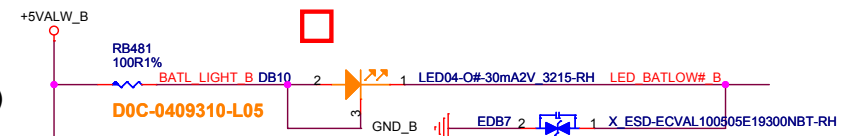
BLUE  
(HDD)



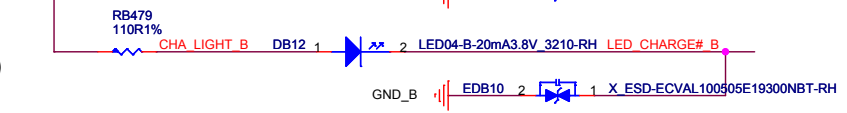
BLUE  
(WLAN)



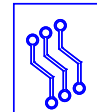
ORANGE  
(BATLOW)



BLUE  
(CHARGE)



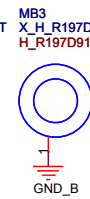
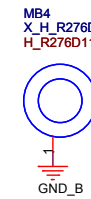
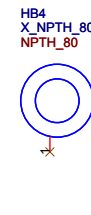
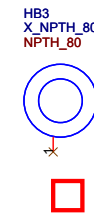
PCBB1



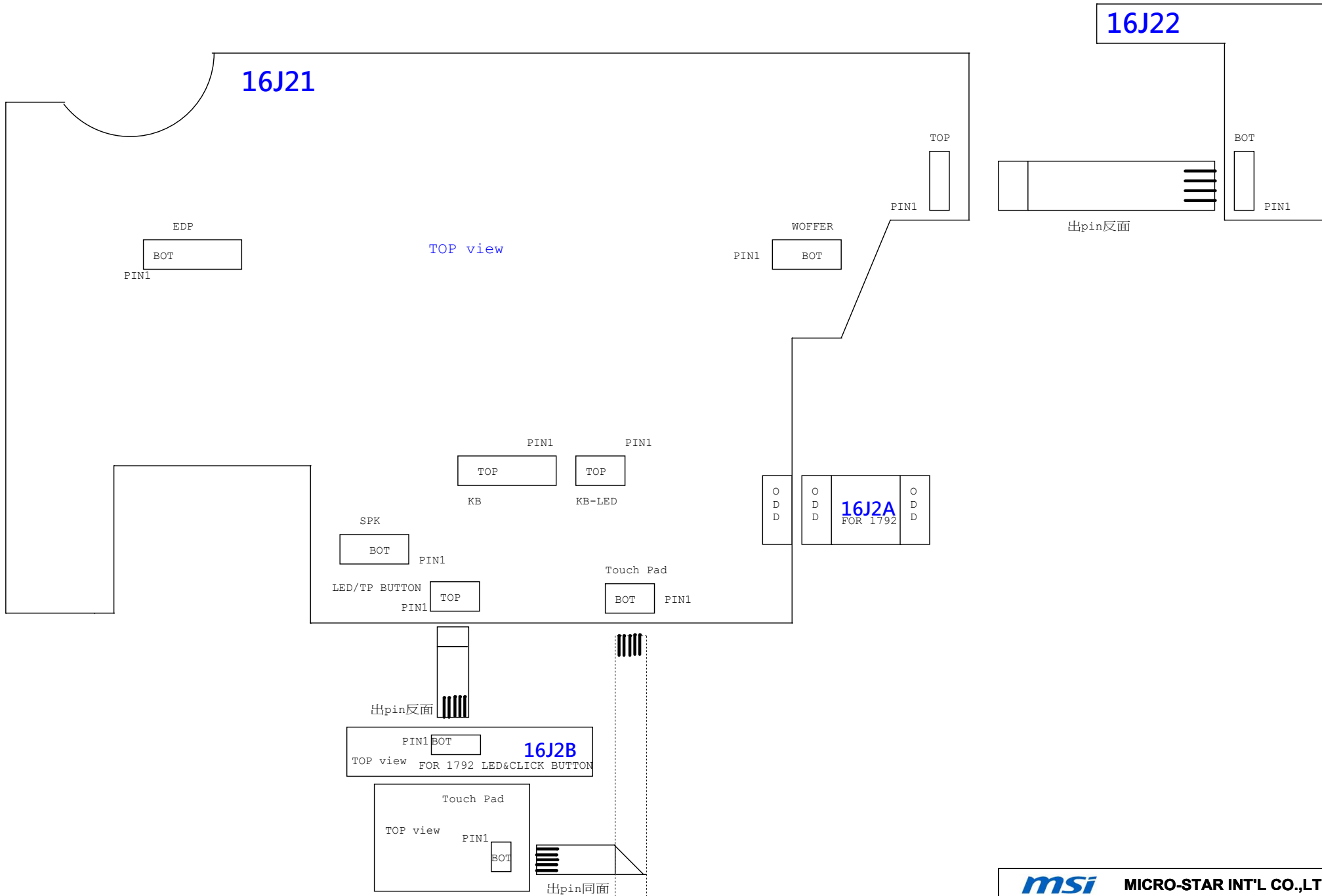
P30-16J2B10-H73

P30-16J2B10-H73

Hannstar: P30-16J2B10-H73  
TRIPOD: P30-16J2B10-T53

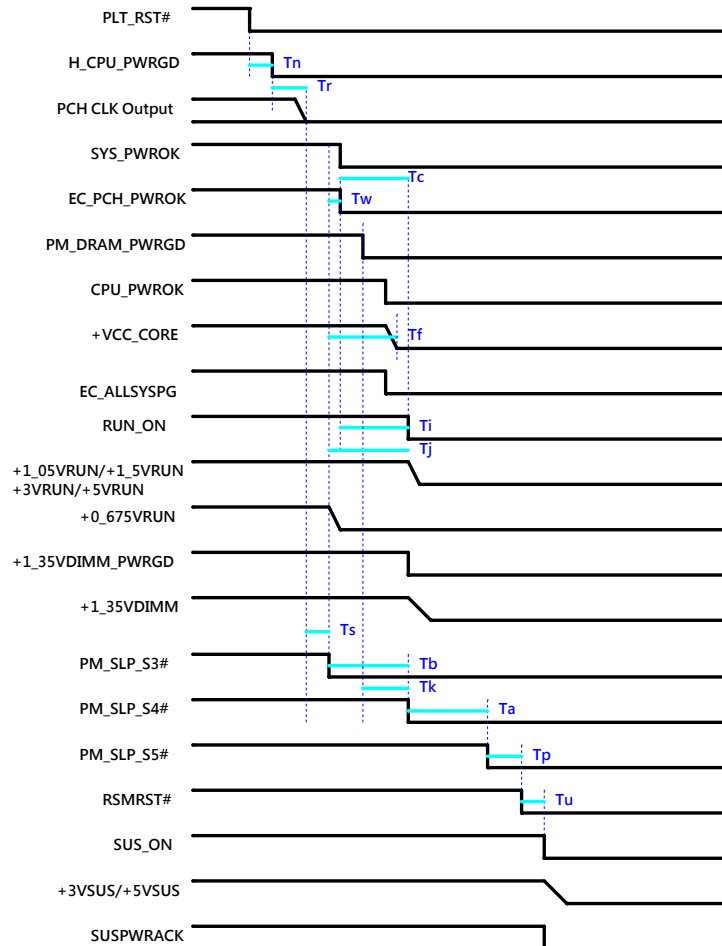


<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title	
<b>[B] 1792 LED/ TP</b>	
Size	Document Number
B	<b>MS-16J2B</b>
Date:	Thursday, November 27, 2014
Sheet	55 of 59
Rev	10



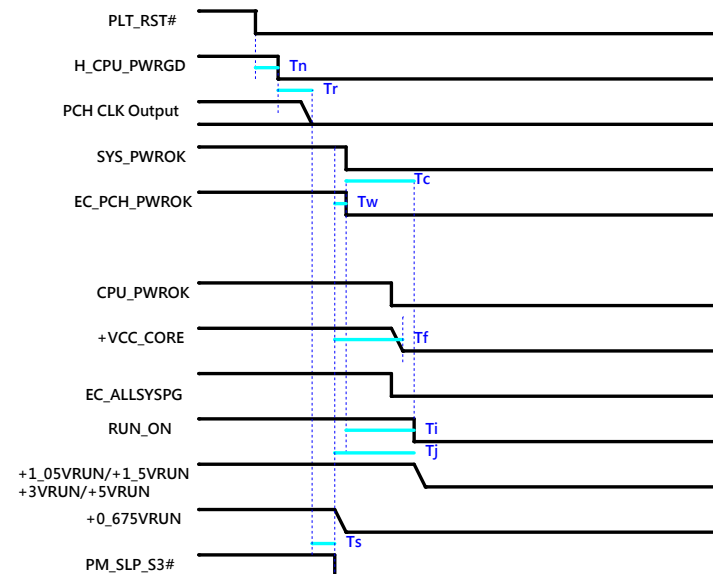
## Power down Sequence

### S0 -> G3



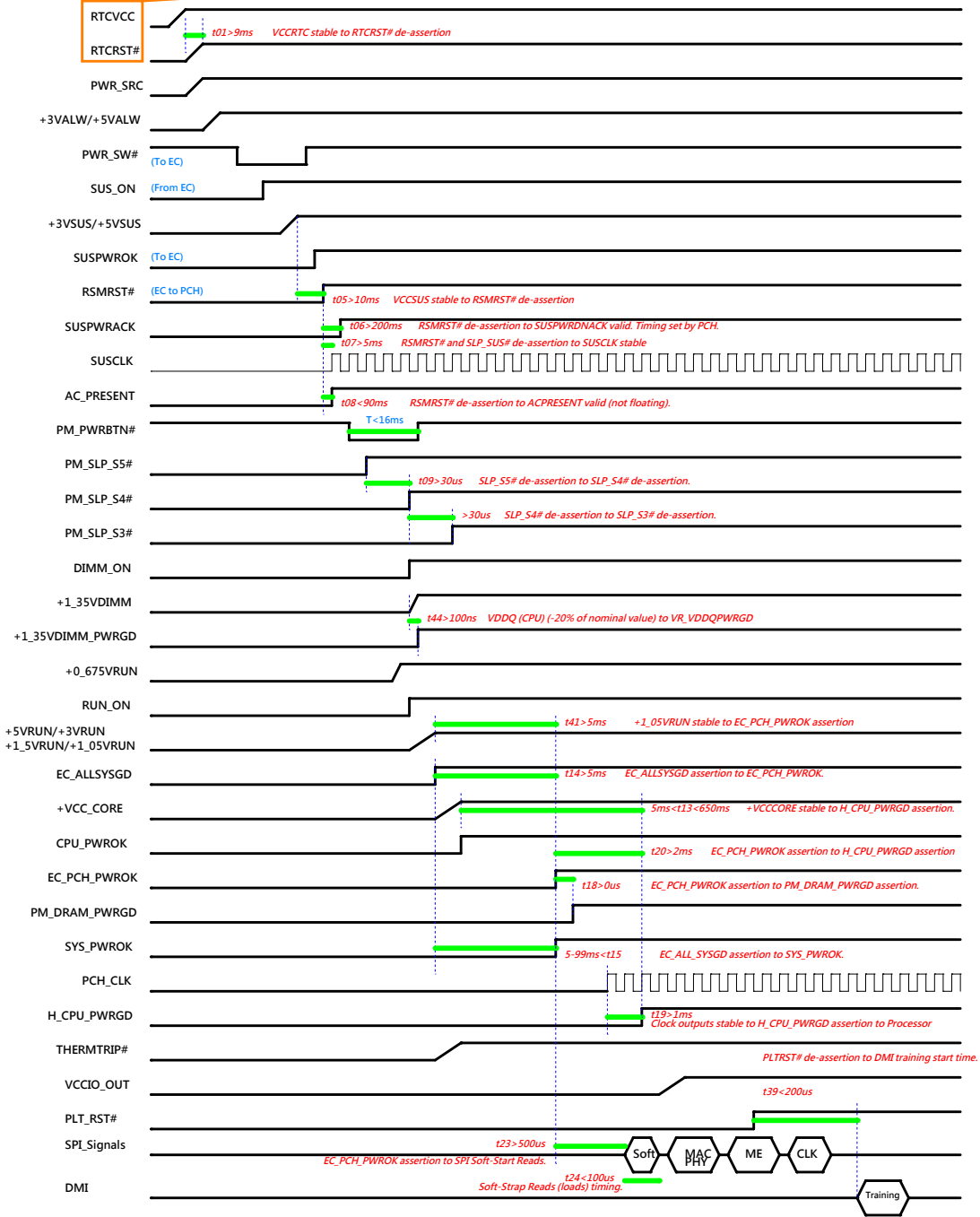
	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

### S0 -> S3

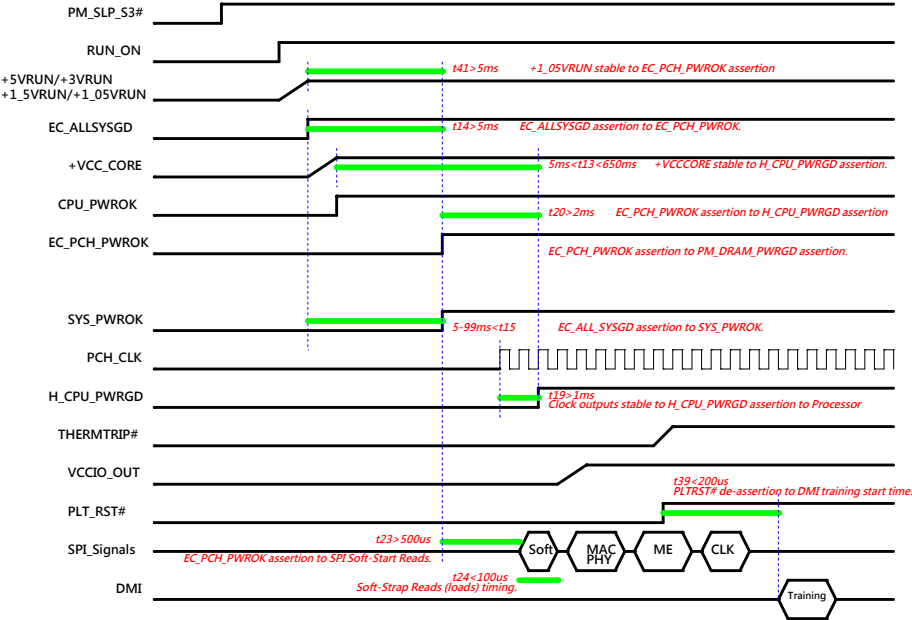


Power on Sequence

G3 -> S0



S3 -> S0



History

0A		0A		10	
Page	Description	Page	Description	Page	Description
21	change U8 from I36-3512A09-A30 to I36-0351109-A30 to reduce softstart time to 400uS	21	change C354 from C11-1063034-W08 to C11-1062314-M09	53	ME change UME11 from E2P-6J11411-G40 to E2P-6J11411-Y42
19	modify GPU GPIO setting to follow design guide	53	MH7 change to connect with GND	53	ME change UME14 from E23-1047010-G40 to E2M-3570611-Y42
18	modify STRAP pin power from 3V3_NV to 3V3_AON (refer to CRB)	59	use MS-16J2_0A_0928B2.upd to update material	50	power modify for GPU power setting PR52,PR56: 39K ohm to 20K ohm PR53: 1.5K ohm to 2K ohm PR54: 30K ohm to 18K ohm PR121: 1.5K ohm to 0 ohm PC45: 1.5nF to 2.7nF
11	G3000 update to formal P/N OB3-AE6B101	53	add UME7 and UME8 for LED sponge	53	ME add UME15,UME16 for 16J2
18	modify GPU strap pin R value to follow CRB	58	update schematics description	43,44	ME change H3,H4 from E2B-1781010-A89 to E2B-16J1010-A89
11	delete R3085 and R3092 for useless (delete signals GFX_REFCLK1 and GFX_REFCLK1#)	50	change PWR_SRC_NVVDD to PWR_SRC	33	delete C805, R434 unstuff, add U36 and C353 for LED KB add TFJUNC29,TFJUNC45,TFJUNC46
13	R3170,R3171,R3172,C3315,C3276 change to unstuff to follow CRB and design guide	53	remove Q3003,Q3099 and connect PEX_CLKREQ# to Q3008	21	R352 change to connect with +3VSUS for signal modify
14	R3169,R3175,R3180,C3277,C3318 change to unstuff to follow CRB and design guide	18	C3438,C3439 change to 18pF	49	PC2 change to 100pF and stuff for signal modify
15	R3057,R3064,R3068,C3057,C3058 change to unstuff to follow CRB and design guide	20	C3237 change to 1uF	34	add C1 and C2 for SA
16	R3139,R3141,R3142,C3258,C3263 change to unstuff to follow CRB and design guide	17,19	add R292,R293,R294,R295,R296,R297	11~20	update GPU P/N to B03-0N16P25-N08 (formal)
13~16	delete net from VFP01_UNC to VFP16_UNC for useless	44	SW1 and SW2 change to N71-0101630-D02 to fix ME problem	18	C3438 and C3439 change to 27pF for SA
50	delete net ISEN3_VGA and PR114 for useless	44,55	modify SW1,SW2,SWB3,SWB4	23	C418 and C419 change to 27pF for SA
34	add net EC_PROTECT_PWR	19	change C3090,C3109,C3170,C3206,C3208 to 4.7uF to follow NVIDIA suggestion	33	C749 and C750 change to 15pF for SA
19	GPU I2CS interface connect with 3V3_AON	52	delete useless impedance line	19	add C3 for signal modify
49~50	change PWR_SRC_FEVDDQ,PWR_SRC_NVVDD to PWR_SRC	39	reserve C488,C489 to connect GND with AGND	16	EC3009 change to unstuff
52	delete EC2,EC21,EC22,EC29 for useless	52	reserve EC16,EC21 to connect PWR_SRC with GND	46~51	delete G1-G17,G19,G20,G21,G22
19	add R3263	34	SW5 change to unstuff	50	PEC3 and PEC6 change to unstuff
52	fix impedance	2	Add compare list for BOM	53~55	update PCB version and information
20	add JNC24	39	delete JNC15 and R203, add C490 and C491 by vendor suggestion	41	change LAN cap from C11-1057612-Y01 to C11-1057412-M09 change LAN cap from C11-1042812-Y01 to C11-1042042-W08
19	R3274 change from 10K to 100K to follow design guide	32	modify eDP pin define	42	delete UME9 and UME10
21	delete PQ46 and R373 for useless	13~16	change C3514,C3293,C3278,C3288,C3307,C3294,C3289,C3122,C3175,C3176,C3177,C3239,C3197,C3195 from C11-4767314-T34 to C11-1062314-M09	53	delete UME15 and UME16
21	delete PQ47,PQ48(D03-0700299-F09) and add PQ55(D03-7002D10-D07)	2	update compare list for BOM	53	Add UME17 for 16J2 ME
21	change PQ7 from D03-0700299-F09 to D03-7002D10-D07	ALL	update 5010/5020	39	Add R106 and R107 for current return path
21	change PC118 footprint from C0603 to C0402	33	C805 unstuff	3~8	CPU P/N: A13-2620135-I06
39	J1 change to connect with GND	2	update compare list for BOM (Add Micron in AVL)	ALL	update 5010/5020
24	change U34 from socket to BIOS ROM	42	ME add HDD sponge UME9,UME10	44	R481 change to 110 ohm R77,R479,R480,R482 change to 100 ohm
11~21	change Cap from 0805 to 0603 (C3065,C3075,C3187,C3259,C3448,C3455,C3064,C3074,C3218,C3435,C3450,C3451)	53	ME add HIDE_GAP_MYLAR UME11	55	RB481 change to 110 ohm RB77,RB479,RB480,RB482 change to 100 ohm
11~21	change Cap from X5R to X6S (C3113,C3121,C3123,C3124,C3128,C3221,C3223,C3225,C3228)	53	EMI add USB3_CON_MYLAR UME12		
11~21	change Cap from X5R to X6S (C3310,C3314,C3308,C3312,C3513,C3179,C3182,C3193,C3222)				